SKB503 Multiprotocol Bluetooth 5/ANT Module Datasheet

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Contents

1 General Description

Ready for Bluetooth 5 and high grade IoT security

The SKB503 is an advanced, highly flexible single chip solution for today's increasingly demanding ULP wireless applications for connected devices on our person, connected living environments and the IoT at large. It is designed ready for the major feature advancements of Bluetooth® 5 and takes advantage of Bluetooth 5's increased performance capabilities which include long range and high throughput modes. Inherent industry-grade security is essential in today's applications.

Bluetooth 5 – Bluetooth low energy further and faster

The SKB503 is ready to take advantage of the considerable performance improvements for Bluetooth low energy with the arrival of the Bluetooth 5 specification. Of greatest importance is the support for longer range (up to x4 compared to Bluetooth 4.x) and doubling of on-air data-rate, up to 2Mbs from 1Mbs in Bluetooth 4.x

Wide protocol support with addition of 802.15.4

The 802.15.4 PHY and MAC layers are supported natively on the SKB503. This allows nRF52840 to be used in a wide range of home and industrial sensor network applications as it supports two of the most popular wireless sensor standards in use today, Bluetooth low energy and 802.15.4 derivatives. This adds to the already existing radio support for Bluetooth low energy, ANT/ANT+ and 2.4GHz for proprietary.

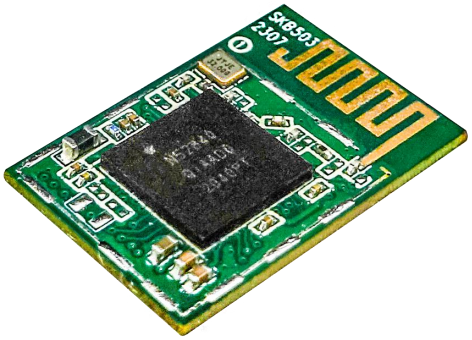

Figure 1: SKB503 Top View

2 Applications

- ◆ Computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad
- ◆ Interactive entertainment devices
  - Remote control
  - 3D Glasses
  - Gaming controller

- Advanced wearables
  - Connected watches
  - Advanced personal fitness devices
  - Wearables with wireless payment
  - Connected Health
  - Virtual/Augmented Reality applications
- IoT
  - Smart Home sensors and controllers
  - Industrial IoT sensors and controllers

3 Features

- Bluetooth 5 ready multi-protocol radio
- Bluetooth 5 data rate support: 2Mbs, 1Mbs, 500Kbs, 125Kbs
- Support ANT Protocol
- 32-bit ARM Cortex-M4F @ 64MHz
- Up to 111 dB link budget for Bluetooth long range mode
- NFC-A on-chip
- Programmable output power from +8dBm to -20dBm
- -96dBm Sensitivity for Bluetooth low energy
- RSSI
- Wide supply voltage range 1.7V to 5.5V
- Full selection of interfaces SPI/UART/PWM
- Programmable Peripheral Interface - PPI
- High speed SPI interface 32MHz
- EasyDMA for all digital interfaces
- 12bit/200K SPS ADC
- 128 bit AES/ECB/CCM/AAR co-processor
- 20 General Purpose I/O pins
- SPI Master/Slave
- Two-wire Master (I2C compatible)
- UART (CTS/RTS)
- RoHS compliance (Lead-free)
- FCC,CE compliance

4 Application Block Diagram

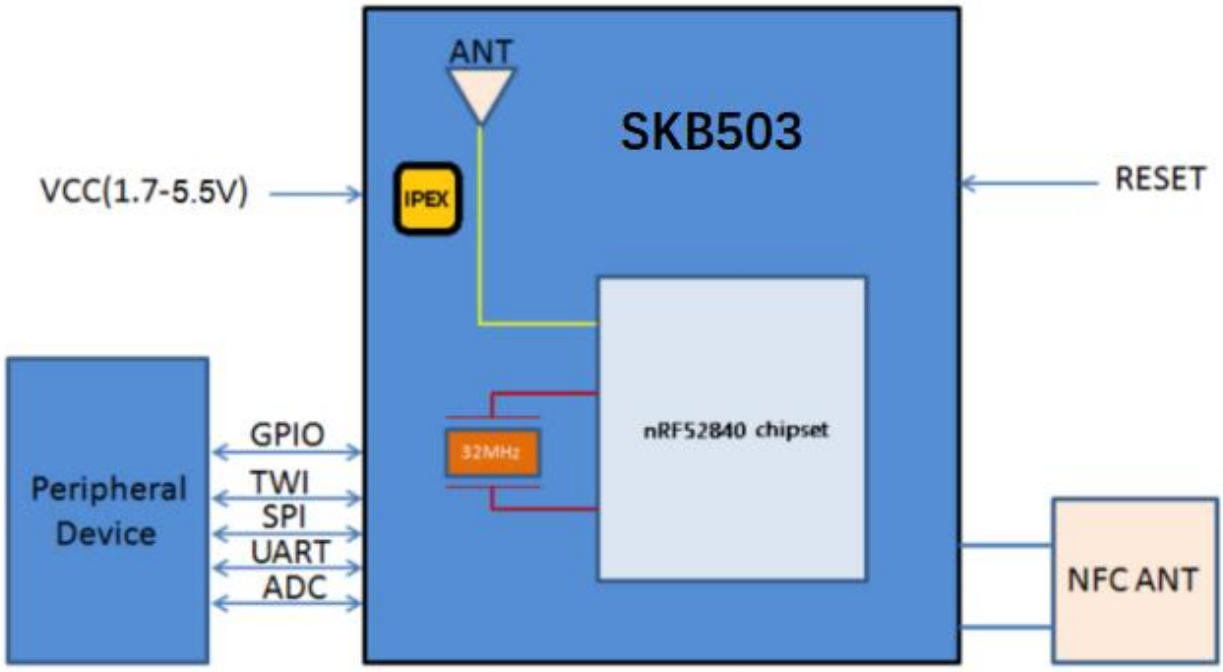

Figure 2: SKB503 Block Diagram

5 Interfaces

5.1 Power Supply

Regulated power for the SKB503 is required. The input voltage of VDD/VDDH range should be 1.7V to 3.6V/2.5~5.5V. Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

5.2 System Function Interfaces

5.2.1 GPIOs

The general purpose I/O is organized as one port with up to 20 I/Os enabling access and control of up to 19 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

1、Input/output direction

2、Output drive strength

3、Internal pull-up and pull-down resistors

4、Wake-up from high or low level triggers on all pins

5、Trigger interrupt on all pins

6、All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels

7、All pins can be individually configured to carry serial interface or quadrature demodulator signals

8、All pins can be configured as PWM signal.

9、There are 6 ADC/LPCOMP input in the 20 I/Os.

5.2.2 Two-wire Interface (I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100kbps ,250kbps and 400kbps. The module has 2 TWI ports and they properties like following table.

Table5-1: TWI Pin Share Scheme

Instance	Master/Slave
TWI0	Master
TWI1	Master

Note： I2C:Inter－Integrated Circuit

5.2.3 Flash Program I/Os

The module has two programmer pins, respectively SWDCLK pin and SWDIO pin. The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

5.2.4 Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The GPIOs are used for each

SPI interface line can be chosen from any GPIOs on the device and configed independently. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

The SPI peripheral support SPI mode 0,1,2,and 3.The module have 3 SPI ports and theirs they properties are as below:

Table5-2: SPI Properties

Instance	Master/Slave
SPI0	Master
SPI1	Master
SPIS1	Slave

5.2.5 UARTs

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS), support in hardware up to 1 Mbps baud. Parity checking is supported.

Support the following baud rate in bps unit:

1200/2400/4800/9600/14400/19200/28800/38400/57600/76800/115200/230400/250000/460800/921600/1000000.

Note: The GPIOs are used for each SPI/TWI/UART interface line can be chosen from any GPIOs on the device and configured independently.

5.2.6 Analog to Digital Converter (ADC)

The 12 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8,10, and 12 bit).

Note: The ADC module uses the same analog inputs as the LPCOMP module. Only one of the modules can be enabled at the same time.

Table5-3: ADC Pins

SKB503 Pin Number	Pin Number	Description
11	P0.28	Digital I/O; Analog input 4
10	P0.29	Digital I/O; Analog input 5
12	P0.30	Digital I/O; Analog input 6
13	P0.31	Digital I/O; Analog input 7
9	P0.02	Digital I/O; Analog input 0
6	P0.03	Digital I/O; Analog input 1
16	P0.04	Digital I/O; Analog input 2
15	P0.05	Digital I/O; Analog input 3

5.2.7 Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wake up source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

5.2.8 Reset

The reset pin of the SKB503 module is in the internal pull-high state , when the reset pin of the module is input to a low level , the module will be automatically reset .After the reset pin is used , the pa rameters of the current setting will not be ANT .

5.2.9 NFC

The NFC peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106kbps bit rate from the NFC Forum.

With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

Listed here are the main features for the NFC peripheral:

- NFC-A listen mode operation
- 13.56 MHz input frequency

- Bit rate 106kbps
- Wake-on-field low power field detection (SENSE) mode
- Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum
- Programmable frame timing controller
- Integrated automatic collision resolution, CRC and parity functions

Table5-4: ADC Pins

SKB503 Pin Number	Pin Number	Description
55	P0.10	Digital I/O; NFC2
56	P0.09	Digital I/O; NFC1

6 Module Specifications

Hardware Features	
Model	SKB503
Antenna Type	PCB Antenna or IPEX connector
Chipset Solution	nRF52840
Voltage	1.7V~5.5V
Dimension(L×W×H)	18.5×12.5×2.0 mm
Wireless Features	
Wireless Standards	Bluetooth ® 5.0，ANT
Frequency Range	2400MHz---2483.5MHz
Data Rates	Uncoded:1Mbps/2Mbps,Coded:125kbps(S=8)/500kbps(S=2)
Modulation Technique	GFSK Modulation
Wireless Security	AES HW Encryption
Transmit Power	Tx Power -20 to +8dBm in 4dB Steps
Work Mode	Central/Peripheral
Others	
Certification	RoHS
Environment	Operating Temperature: -40℃~85℃
	Storage Temperature: -40℃~125℃
	Operating Humidity: 10%~90% Non-condensing

	Storage Humidity: 5%~90% Non-condensing

7 Module Pinout and Pin Description

7.1 Module Pinout

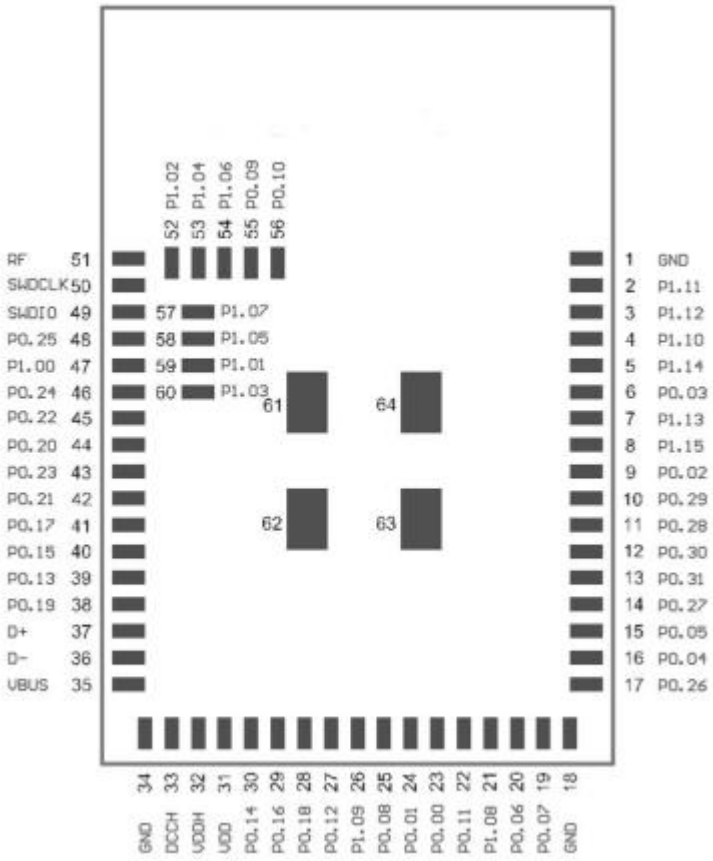

Figure 3: SKB503 Module Pinout

7.2 Pin Description

Pin No.	Pin Name	Description	Remark
1	GND	Power	Ground
2	P1.11	Digital I/O	General purpose I/O
3	P1.12	Digital I/O	General purpose I/O
4	P1.10	Digital I/O	General purpose I/O
5	P1.14	Digital I/O	General purpose I/O
6	P0.03：AIN1	Digital I/O；Analog input	General purpose I/O；Analog input
7	P1.13	Digital I/O	General purpose I/O
8	P1.15	Digital I/O	General purpose I/O

9	P0.02；AIN0	Digital I/O；Analog input	General purpose I/O；Analog input
10	P0.29	Digital I/O	General purpose I/O
11	P0.28；AIN4	Digital I/O；Analog input	General purpose I/O；Analog input
12	P0.30；AIN6	Digital I/O；Analog input	General purpose I/O；Analog input
13	P0.31；AIN7	Digital I/O；Analog input	General purpose I/O；Analog input
14	P0.27	Digital I/O	General purpose I/O
15	P0.05	Digital I/O	General purpose I/O
16	P0.04；AIN2	Digital I/O；Analog input	General purpose I/O；Analog input
17	P0.26	Digital I/O	General purpose I/O
18	GND	Power	Ground
19	P0.07	Digital I/O	General purpose I/O
20	P0.06	Digital I/O	General purpose I/O
21	P1.08	Digital I/O	General purpose I/O
22	P0.11；TRACEDAT	Digital I/O；Trace data	General purpose I/O； Trace buffer TRACEDATA[2]
23	P0.00；XL1	Digital I/O；Analog input	General purpose I/O； Connection for 32.768 kHz crystal
24	P0.01；XL2	Digital I/O；Analog input	General purpose I/O； Connection for 32.768 kHz crystal
25	P0.08	Digital I/O	General purpose I/O
26	P1.09；TRACEDATA3	Digital I/O；Trace data	General purpose I/O； Trace buffer TRACEDATA[3]
27	P0.12；TRACEDATA1	Digital I/O；Trace data	General purpose I/O； Trace buffer TRACEDATA[1]
28	P0.18；nRESET	Digital I/O	General purpose I/O； Configurable as pin RESET
29	P0.16	Digital I/O	General purpose I/O
30	P0.14	Digital I/O	General purpose I/O
31	VDD	Power	Power supply, 1.7V-3.6V

32	VDDH	Power	Power supply, 2.5V-5.5V
33	DCCH	Power	DC/DC converter output
34	GND	Power	Ground
35	VBUS	Power	USB Power Supply, 4.35V-5.5V
36	D-	Digital I/O	USB D-
37	D+	Digital I/O	USB D+
38	P0.19	Digital I/O	General purpose I/O
39	P0.13	Digital I/O	General purpose I/O
40	P0.15	Digital I/O	General purpose I/O
41	P0.17	Digital I/O	General purpose I/O
42	P0.21	Digital I/O	General purpose I/O
43	P0.23	Digital I/O	General purpose I/O
44	P0.20	Digital I/O	General purpose I/O
45	P0.22	Digital I/O	General purpose I/O
46	P0.24	Digital I/O	General purpose I/O
47	P1.00;TRACEDATA0	Digital I/O;Trace data	General purpose I/O； Trace buffer TRACEDATA[0]
48	P0.25	Digital I/O	General purpose I/O
49	SWDIO	Debug	Debug serial data
50	SWDCLK	Debug	Serial wire debug clock input for debug and programming
51	RF	RF	Single-ended radio antenna connection
52	P1.02	Digital I/O	General purpose I/O
53	P1.04	Digital I/O	General purpose I/O
54	P1.06	Digital I/O	General purpose I/O
55	P0.09；NFC1	Digital I/O；NFC input	General purpose I/O； NFC antenna connection

56	P0.10；NFC2	Digital I/O；NFC input	General purpose I/O； NFC antenna connection
57	P1.07	Digital I/O	General purpose I/O
58	P1.05	Digital I/O	General purpose I/O
59	P1.01	Digital I/O	General purpose I/O
60	P1.03	Digital I/O	General purpose I/O
61	GND	Power	Ground
62	GND	Power	Ground
63	GND	Power	Ground
64	GND	Power	Ground

8 PCB Design Guide

Please reserve empty area for PCB Antenna when you are going to aboard, device's the empty range design minimum size :12.5*4.55mm , please kindly check the "PCB footprint and Dimensions" for refere nce.

9 PCB Footprint and Dimensions

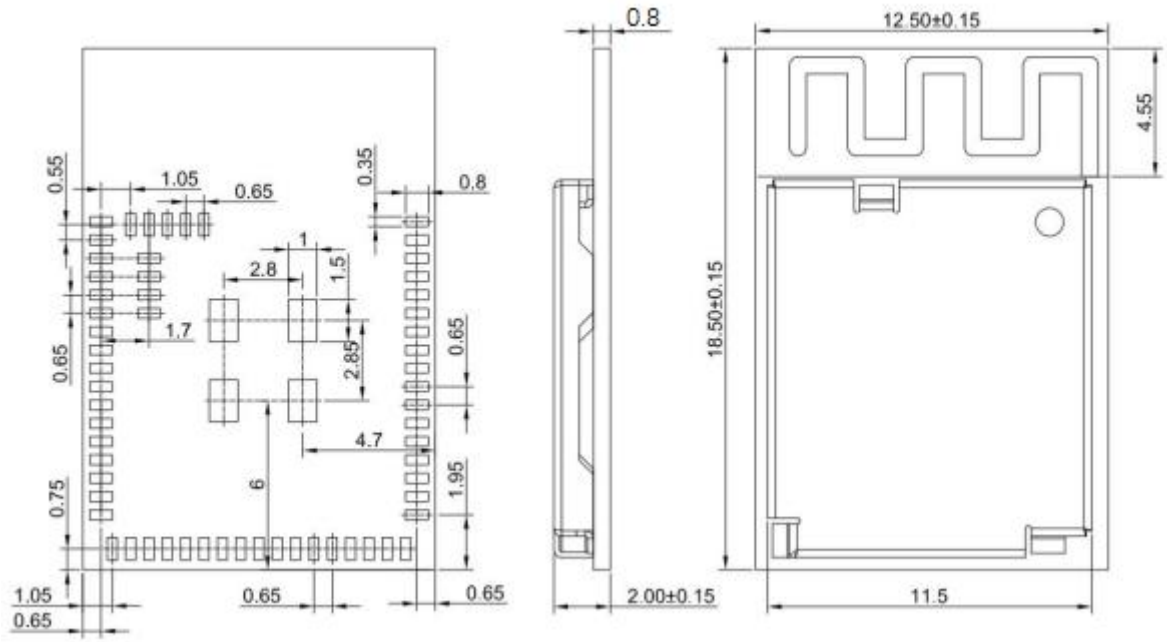

Figure 4: SKB503 Recommended PCB Footprint

10 Electrical Characteristics

10.1 Absolute Maximum Ratings

Table10-1: Absolute Maximum Ratings

Parameter	Condition	Min.	Typ.	Max.	Unit
Storage Temperature Range		-40		125	°C
ESD Protection	VESD	/		4000	V
Supply Voltage	VCC	-0.3		3.9	V
Voltage On Any I/O Pin		-0.3		3.63	V

*SKB503 series modules are Electrostatic Sensitive Devices and require special precautions while handling.

ESD precautions

The SKB503 series modules contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Handling the SKB503 series modules without proper ESD protection may destroy or damage them permanently.

The SKB503 series modules are electrostatic sensitive devices (ESD) and require special ESD precautions typically applied to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling, transportation and operation of any application that incorporates the SKB503 series module. Don't touch the module by hand or solder with non-anti-static soldering iron to avoid damage to the mod

10.2 Recommended Operation Ratings

Table10-2: Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Extended Temp. Range	TA	-40	25	85	ºC

Power Supply	VDD	1.7	3.3	3.6	V
Power Supply	VDDH	2.5	5	5.5	V
Input Low Voltage	VIL	0		0.3*VDD	V
Input High Voltage	VIH	0.7*VDD		VDD	V

10.3 Current

Table10-3: Power Consumption in Different States

System State	TX Peak@4dBm	RX Peak	Sleep Mode（avg）	Idle Mode (avg)
Current (peak)@VDD=3V	7.5mA	5.4mA	0.4uA	1.2uA

11 Manufacturing Process Recommendations

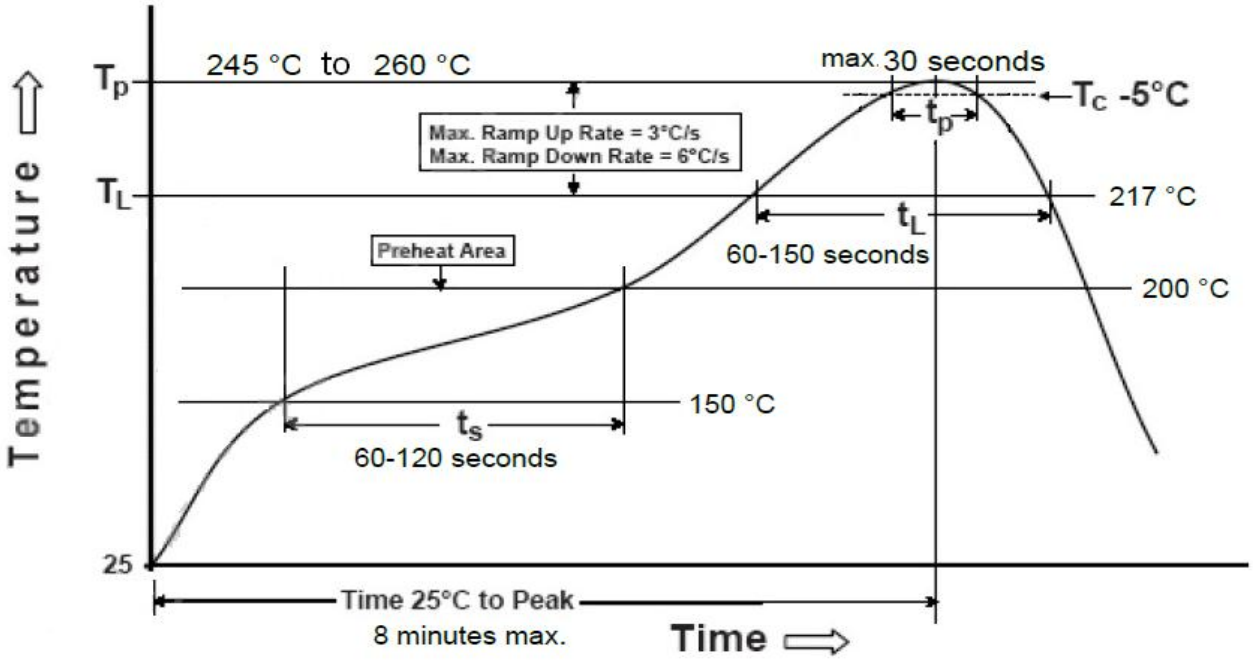

Figure 5: SKB503 Typical Lead-free Soldering Profile

Note： The final re-flow soldering temperature map chosen at the factory depends on additional external factors, for example, choice of soldering paste, size, thickness and properties of the module's baseboard etc. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

12 Packaging Specification

SKB503 modules are put into tray and 528 units per tray. Each tray is 'dry' and vacuum packaging.

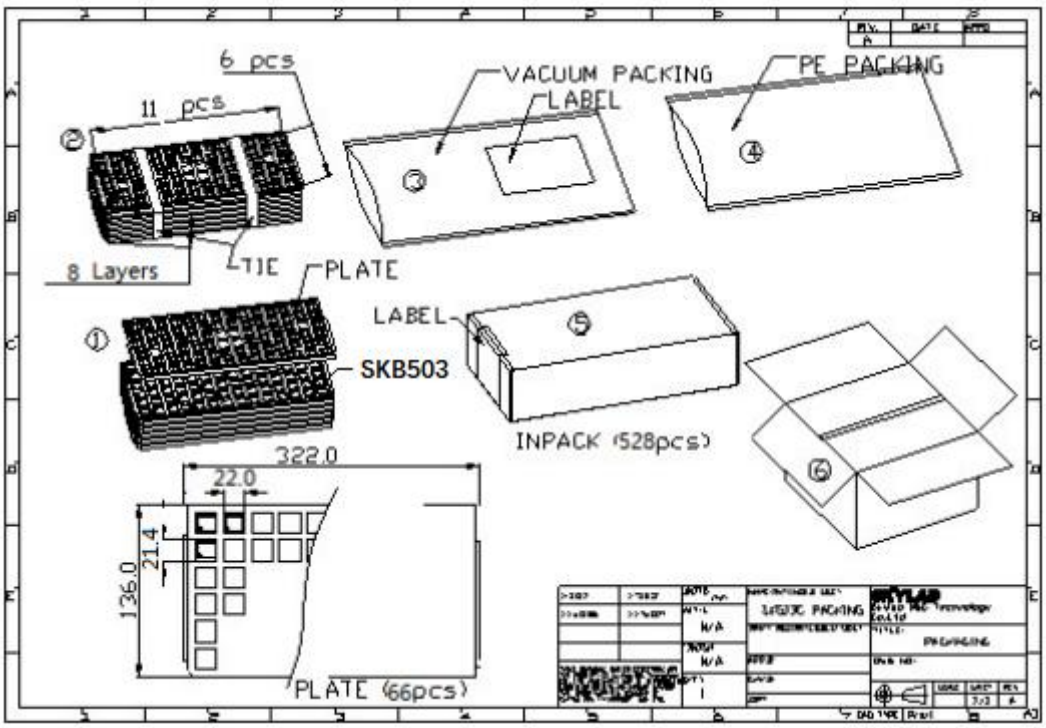

Figure 6: SKB503 Packaging

13 Ordering Information

Module No.	Crystal	Shielding	Antenna	Temperature Grade
SKB503-CSPI	32.768K	Shielding	PCB	Industry
SKB503-XXPI	No	No	PCB	Industry

14 Contact Information

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