# SKB380 规格书
# 蓝牙5.0 模组/
# SKB380 Datasheet
# BLE 5.0 Module

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# 目录 Contents

# 1. 产品介绍/ Product Introduction

SKB380 模块是一个高度集成的蓝牙 5.0 低功耗（BLE）单模蓝牙模块。模块自带 ARM Cortex-M0 32 位处理器，512KB Flash，64KB SRAM，并集成 UART、SPI、I2C、PWM、ADC 等丰富外设。模块拥有尺寸小、功耗低等优点，非常适合智能穿戴设备、智能家居、运动健身设备、消费电子、工业控制等 IOT 应用场景。

The SKB380 module is a highly integrated Bluetooth 5.0 low power (BLE) single-mode Bluetooth module. The module comes with ARM Cortex-M0 32-bit processor, 512KB Flash, 64KB SRAM. It integrates UART, SPI, I2C, PWM, ADC and other rich peripherals. The module has the advantages of small size and low power consumption, which is very suitable for IOT application scenarios such as smart wearable devices, smart homes, sports and fitness equipment, consumer electronics, and industrial control.

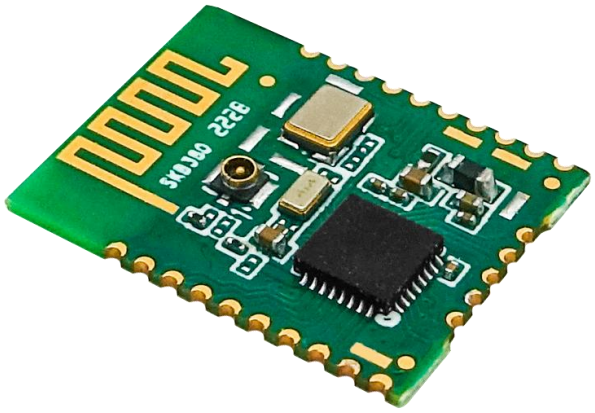

**Figure 1: SKB380 product picture**

# 2. 特点/ Features

- 蓝牙低功耗 BLE 5.0 协议/ Bluetooth® 5.0 low energy
- 支持串口到蓝牙透传/ Support UART-to-BLE transparent transmission.
- 支持 BLE 速率模式/ Supported BLE data rates : 1Mbps, 2Mbps
- 6 路 24 位定时器，支持 RTC/ 6x24bit timers, RTC support
- 支持 6 通道 PWM/ Support up to 6 channel PWM
- 3 路 12 位 ADC 检测功能/ 12bit ADC and 3 configurable channels
- 19*GPIO, 2*SPI, 2*I2C,
- 1 路 PGA，支持模拟麦克风输入/ 1*PGA, support microphone analog input
- 兼容 ROHS（无铅）/ ROHS compliance (Lead-free)

# 3. 应用场景/ Applications

- 电脑输入输出外设/ Computer peripherals and I/O devices
  - 鼠标/ Mouse
  - 键盘/ Keyboard
  - 多点触控板/ Multi-touch trackpad
- 交互式娱乐设备/ Interactive entertainment devices
  - 遥控器/ Remote controller
  - 3D 眼镜/ 3D Glasses
  - 游戏控制器/ Gaming controller
- 个人局域网/ Personal Area Networks
  - 健康传感及监控设备/ Health/fitness sensor and monitor devices
  - 医疗设备/ Medical devices
  - 遥控钥匙+手表手环/ Key-fobs + wrist watches
- 遥控玩具/Remote control toys
- 室内定位蓝牙信标/Indoor Location Beacons
- 彩色遥控 LED 灯/Colourful LED Control
- 楼宇自动化/Building automation
- 传感器网络/Sensor networks.
- 资产追踪/Asset tracking.

# 4. 应用框图/Application Block Diagram

SKB380 模组内部集成 1.1V DCDC，默认贴 32.768kHz 晶体和 16MHz 晶体。

SKB380 module integrates 1.1V DCDC. The 32.768kHz and 16MHz crystal is default mounted.

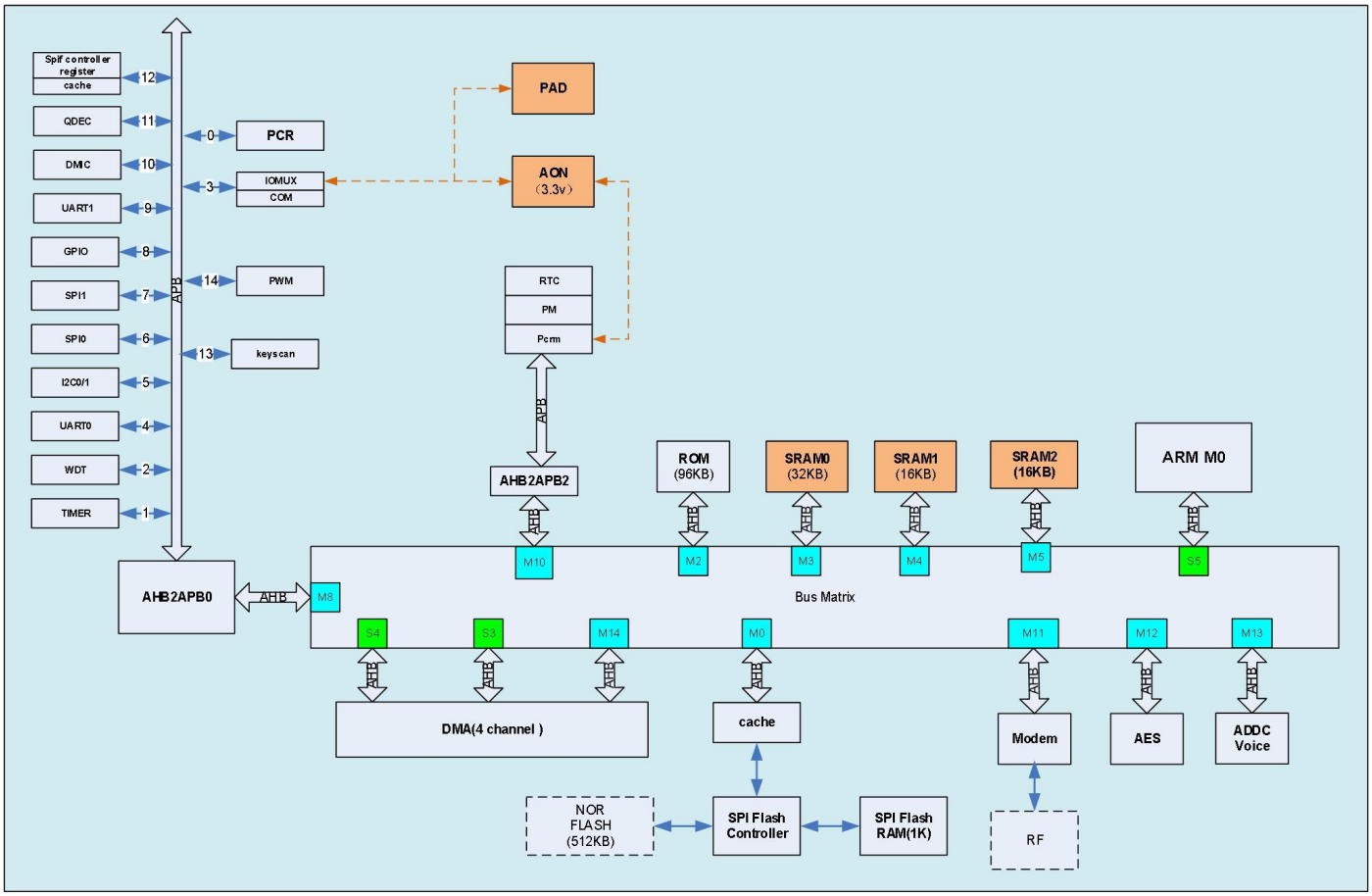


**Figure 4: SKB380 Block Diagram**

# 5. 管脚定义/Pinout Description

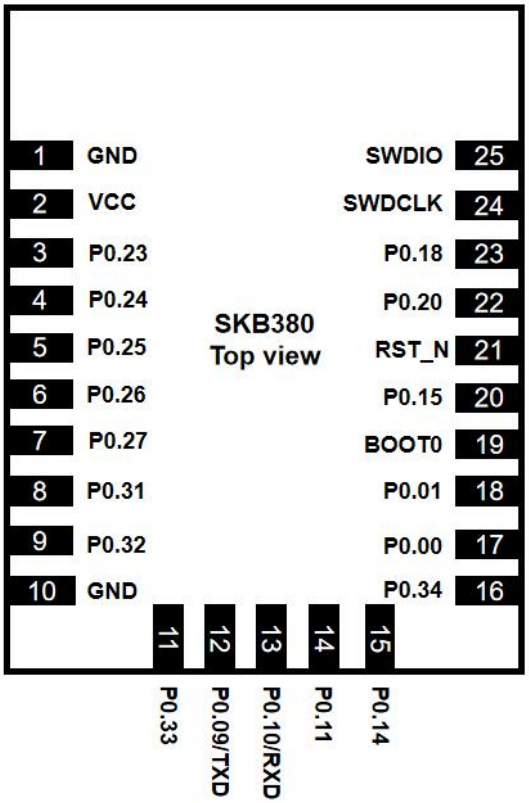


**Figure 5: SKB380 引脚图/SKB380 Module Pinout**

| 引脚/ Pin No. | 引脚名称/ Pin Name | 引脚类型/Pin type | 备注/Remark |
|---|---|---|---|
| 1 | GND | Ground | 接地焊盘/Ground PAD |
| 2 | VCC | Power Supply | 1.8~3.6V 电源供电脚，使用一个 10uF 和一个 0.1uF 滤波电容靠近 1 脚和 2 脚/<br>1.8V to 3.6V power supply,Place a 10uF and a 0.1uF filter capacitors near pin1 and pin2 |
| 3 | P0.23 | Digital I/O | 通用输入/输出端口/General input/output port |
| 4 | P0.24 | Digital I/O | 通用输入/输出端口/General input/output port |
| 5 | P0.25 | Digital I/O | 通用输入/输出端口/General input/output port |
| 6 | P0.26 | Digital I/O; Analog input | 通用输入/输出端口/General input/output port;<br>模数转换输入口/ADC input 4 |
| 7 | P0.27 | Digital I/O; Analog input | 通用输入/输出端口/General input/output port;<br>模数转换输入口/ADC input 5 |

| | | | |
|---|---|---|---|
| 8 | P0.31 | Digital I/O; Analog input | 通用输入/输出端口/General input/output port;<br>模数转换输入口/ADC input 6 |
| 9 | P0.32 | Digital I/O; Analog input | 通用输入/输出端口/General input/output port;<br>模数转换输入口/ADC input 7 |
| 10 | GND | Ground | 接地焊盘/Ground PAD |
| 11 | P0.33 | Digital I/O; Analog input | 通用输入/输出端口/General input/output port;<br>模数转换输入口/ADC input 0 |
| 12 | P0.09/<br>TXD | Digital I/O; Analog input | 通用输入/输出端口/General input/output port;<br>模数转换输入口/ADC input 1<br>**默认串口发送/Default UART TX** |
| 13 | P0.10/<br>RXD | Digital I/O | 通用输入/输出端口/General input/output port<br>电容触控输入 /Cap detection for touch pad input<br>**默认串口接收/Default UART RX** |
| 14 | P0.11 | Digital I/O | 通用输入/输出端口/General input/output port<br>电容触控输入 /Cap detection for touch pad input |
| 15 | P0.14 | Digital I/O | 通用输入/输出端口/General input/output port<br>电容触控输入/Cap detection for touch pad input |
| 16 | P0.34 | Digital I/O | 通用输入/输出端口/General input/output port<br>电容触控输入/ Cap detection for touch pad input |
| 17 | P0.00 | Digital I/O | 通用输入/输出端口/General input/output port |
| 18 | P0.01 | Digital I/O | 通用输入/输出端口/General input/output port |
| 19 | BOOT0 | Digital I | 启动选择 0，高电平上电进入烧录模式或测试模式，默认下拉/<br>Boot_select[0], enter program mode or test mode when high |
| 20 | P0.15 | Digital I/O | 通用输入/输出端口/General input/output port |
| 21 | RST_N | Digital I/O;<br>System Reset | （默认）通用输入/输出端口/（Default）General input/output port<br>（需配置）复位/（Need configuration) Reset |
| 22 | P0.20 | Digital I/O | 通用输入/输出端口/General input/output port |
| 23 | P0.18 | Not Connect | 通用输入/输出端口/General input/output port |
| 24 | SWDCLK | Hardware debug and Flash program | 串行总线调试时钟输入口/SWD(Serial wire debug) clock input |
| 25 | SWDIO | Hardware Debug and Flash Program | 串行总线调试数据 I/O 口/SWD(Serial wire debug) data input and output |

# 6. 功能介绍/Function description

## 6.1 电源、时钟与复位/ Power supply, clock, and reset

**模块具有 2 种低功耗模式/ The module has 2 low power consumption modes：**

**睡眠模式/ Sleep mode**

在 Sleep 模式下，CPU 停止运行，大部分外设寄存器内容丢失并停止工作（除 GPIO 上下拉与唤醒配置、RTC 外），SRAM 内容保持，GPIO 状态保持，RTC 继续运行。通过 RTC 匹配中断、GPIO 中断，可唤醒 CPU。CPU 唤醒后，可直接运行之前加载的 SRAM 代码，无需重新加载代码。/ In Sleep mode, the CPU stops running, most of the peripheral registers will lose their contents and stop working (except GPIO pull-up/down and wake-up configuration, RTC), SRAM content is maintained, GPIO status is maintained, and RTC continues to run. The CPU can be waked by RTC matching interrupt and GPIO interrupt. After the CPU wakes up, it can directly run the previously loaded SRAM code without reloading the code.

**关机模式/OFF mode**

在 OFF 模式下，CPU 停止运行，大部分外设寄存器内容丢失并停止工作（除 GPIO 上下拉与唤醒配置、RTC 外），SRAM 内容丢失，GPIO 状态保持，RTC 停止运行。通过 GPIO 中断，可唤醒 CPU。CPU 唤醒后，将复位重新加载代码运行。

In OFF mode, the CPU stops running, most of the peripheral registers will lose their contents and stop working (except GPIO pull-up/down and wake-up configuration, RTC), SRAM contents are lost, GPIO status is maintained, and RTC stops running. The CPU can be waked by GPIO interrupt. After the CPU wakes up, it will reset and reload the code.

Sleep 模式下功耗比 OFF 模式功耗大，但是 Sleep 模式能够快速唤醒。当模块开启低功耗模式时，在保持蓝牙通信功能正常的情况下，模块将周期性（周期时间约等于广播间隔或连接间隔时间）进入 Sleep 模式，并自动唤醒。

The Sleep mode may wake the CPU up more quickly in spite of its higher power consumption compared with the OFF mode. For the module under the low power consumption mode, it will periodically (approximately at the broadcast interval or connection interval) enter the Sleep mode and automatically wake up while maintaining the normal Bluetooth communication function.

模块时钟系统包含高速时钟源与低速时钟源，高速时钟源用于 CPU 以及大部分外设，低速时钟源用于 RTC 。整个模块包含下列时钟：

The module clock system includes a high-speed clock source and a low-speed clock source. The former is used for the CPU and most peripherals, and the latter is used for RTC. The entire module contains the following clocks：

- 32MHz 内部高速 RC 振荡器，校准后精度 3%/ 32MHz internal high-speed RC oscillator with 3% accuracy after calibrating
- 32KHz 内部低速 RC 振荡器，校准后精度 500ppm/ 32KHz internal low-speed RC oscillator with 500ppm accuracy after calibrating
- 16MHz 高速晶体振荡器/ 16MHz high-speed crystal oscillator
- 32.768Hz 低速晶体振荡器/ 32.768Hz low-speed crystal oscillator
- 倍乘系数为 2,3,4 的 DLL&DBL 锁相环（16MHz 高速时钟进行倍频）/ DLL&DBL phase-locked loop with multiplication factor of 2,3,4 (for frequency multiplication of 16MHz high-speed clock)
- 当采用 32KHz 内部低速 RC 振荡器作为系统低速时钟源时，模块将定时采用 16M 晶振高速时钟对其进行校准，使 RC32K 振荡器的频率为 32.768KHz。/ If the 32KHz internal low-speed RC oscillator serves as the system low-speed clock source, the module will regularly calibrate it with a 16M crystal oscillator high-speed clock to ensure that the frequency of RC32K oscillator is kept at 32.768KHz.

时钟系统如图 6-1 所示。CPU 支持的时钟源为/ The clock system is shown in Figure 6-1. The clock sources supported by the CPU are：

- 16MHz 晶振时钟/ 16MHz crystal clock
- 48MHz 晶振倍频时钟/ 48MHz crystal DLL clock
- 64MHz 晶振倍频时钟/ 64MHz crystal DLL clock
- 32MHz RC 振荡器时钟（该时钟源下 RF 无法正常工作）/ 32MHz RC oscillator clock(The RF can’t work under this clock source)

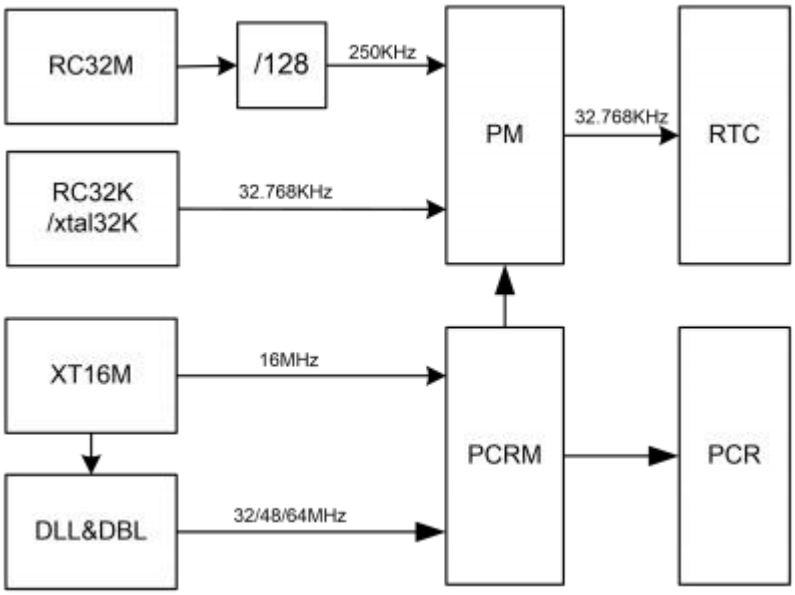


**图 6-1 时钟系统/ Clock system**

模块外设具有独立的复位功能，通过控制寄存器，可实现外设的复位。

With independent reset function, the module peripherals may be reset through the control register.

模块复位引脚可实现整个模块的硬件复位，复位引脚内部集成 120KΩ上拉电阻。复位信号低电平有效。

The module reset pin, which integrates a 120KΩ pull-up resistor internally, can realize the hardware reset of the entire module. The reset signal is active low.

## 6.2 接口介绍/ Interface introduction

### 6.2.1 GPIO

模块提供 20/9 个 GPIO，每个 GPIO 引脚都可以由软件配置成输入、输出或大部分数字外设功能端口。GPIO 特性如下：

The module provides 20/ 11 GPIOs, and each GPIO pin can be configured by software as input, output or most digital peripheral function ports. GPIO characteristics are as follows：

- 每个 GPIO 可以配置其上下拉电阻，可供选择的上下拉电阻参数为/ Each GPIO can be configured with its pull-up/down resistance, and the available pull-up/down resistance parameters are：
  - ✓ 浮空，高阻态/Floating, high impedance
  - ✓ 强上拉，上拉电阻约 150KΩ/ Strong pull-up, with pull-up resistance of about 150KΩ
  - ✓ 弱上拉，上拉电阻约 1MΩ/ Weak pull-up, with pull-up resistance of about 1MΩ
  - ✓ 下拉，下拉电阻约 100KΩ/ Pull-down, with pull-down resistance of about 100KΩ
- 所有 GPIO 可支持唤醒输入，通过配置成上升沿或下降沿，可将模块从 Sleep 模式或 OFF 模式唤

醒。/ All GPIOs support wake-up input, and may be configured as a rising edge or falling edge to wake up the module from Sleep mode or OFF mode.

- 所有 GPIO 支持外部中断输入，可配置成边沿或电平触发中断。边沿触发包含上升沿、下降沿触发，电平触发包含高电平、低电平触发。/ All GPIOs support external interrupt input and can be configured as an edge or level trigger interrupt.

Edge trigger includes rising edge and falling edge trigger, level trigger includes high level and low level trigger

- GPIO 输出状态在 Sleep 模式或 OFF 模式可配置保持。/ GPIO output state can be configured and maintained in Sleep mode or OFF mode
- 当 GPIO 配置成外部唤醒输入时，需要开启内部的上下拉电阻，不能配置为高阻态。/ When the GPIO is configured as an external wake-up input, the internal pull-up/down resistors need to be turned on, and GPIO cannot be configured as a high-impedance state.
  - ✓ 当配置为上升沿唤醒时，需要开启内部下拉电阻/ For configuration of rising edge wake-up, the internal pull-down resistors shall be turned on
  - ✓ 当配置为下降沿唤醒时，需要开启内部上拉电阻/ For configuration of falling edge wake-up, the internal pull-up resistors shall be turned on

上下拉电阻硬件默认值如下/ The hardware default values of the pull-up/down resistors are as follows：

- P03、P24、P25：下拉。/ P03 、P24 、P25: Pull-down
- 其他 GPIO：浮空。/ Other GPIOs: floating.

当 GPIO 做输出时，可配置 retention 功能。retention 默认是关闭的。retention 打开时，系统进入系统休眠后，GPIO 的输出特性和输出值保持不变。retention 关闭时，系统休眠时，GPIO 会恢复默认输入态。

When GPIO serves as an output, retention function can be configured. Retention is off by default. When retention is enabled, the output characteristics and output values of GPIO remain unchanged after the system enters Sleep mode. When retention is disabled, the GPIO will return to the default input state when the system enters Sleep mode.

**注意/ Notes：**

1）P02、P03 引脚上电默认为 SWD 接口。

The P02 and P03 pins are powered on by default as SWD interface.

2）P01 不支持 IOMUX 功能，IOMUX 是指将 GPIO 复用为其他模块引脚。

P01 does not support IOMUX. IOMUX means to reuse GPIO pins to other modules.

3）BOOT0、P24/BOOT1/AIO2、P25/BOOT2/AIO8 引脚决定了模块的工作模式，使用时需注意引脚状态对工作模式的影响。

As BOOT0, P24/BOOT1/AIO2, P25/BOOT2/AIO8 pins determine the working mode of the module, attention must be paid to the influence of the pin status on the working mode.

4）P23 引脚不能接快速变化的信号（包含输入信号与输出信号），信号频率需小于 10KHz，否则将影响 RF 接收。

The P23 pin cannot receive fast-changing signals (including input signals and output signals), and the signal frequency must be less than 10KHz. Otherwise, the RF reception will be affected.

### 6.2.2 UART

通用同步异步收发器为 MCU 和外部器件连续通信提供了一个通用接口。通过 UART 的 2 根信号线，可实现与外部器件的通信。模块提供 UART0 与 UART1 两路 UART 接口。UART 接口特性如下：

The universal synchronous/asynchronous transceiver provides a universal interface for continuous communication between the MCU and external devices through 2 signal lines of UART. The module provides two UART interfaces, UART0 and UART1. The characteristics of UART interface are as follows:

- 全双工异步通信/ Full duplex asynchronous communication
- 可编程波特率，最高波特率为 fsys/16/ Programmable baud rate, with baud rate up to fsys/ 16
- 独立的发送 FIFO 与接收 FIFO，FIFO 深度为 16*8bit/ Independent transmission and reception of FIFO, with FIFO depth of 16*8bit
- 可编程串口特性/ Programmable serial port features
  - ✓ 数据位 5,6,7,8bit 可选/ Optional data bit (5,6,7,8bit)
  - ✓ 奇校验、偶校验、无校验可选/ Optional odd parity, even parity, no parity
  - ✓ 停止位 1bit、1.5bit 或 2bit 可选/ Optional stop bit (1 bit, 1.5 bit or 2 bit)
- 当系统进入 Sleep 时，UART 配置信息将丢失，唤醒后需要重新配置/ Under Sleep mode, the UART configuration information will be lost, and a re-configuration is required upon system wake-up.
- UART 外设引脚可映射至任意 IO 口。模块处于烧录模式下，将采用 UART0 进行通信，此时 UART0 映射至 P09（UART0_TX）、P10（UART0_RX）。/ UART peripheral pins can be mapped to any IO port. Under Programming mode, UART0 is used for communication and will be mapped to P09 (UART0_TX) and P10 (UART0_RX).

### 6.2.3 SPI

模块提供 SPI0 与 SPI1 两个外设接口，两路 SPI 是互斥的，同一时刻只能一路 SPI 通信。该两个外设接口通过 4 线 SPI 方式可以和外部器件通信，其特性如下：

The module provides two peripheral interfaces, SPI0 and SPI1, which can communicate with external devices through 4-wire SPI. SPI wrapper contains one SPI master and one SPI slave. They are logically exclusive. Only one block is alive at a time. Specific features are as follows:

- 支持主机模式与从机模式/ Support master mode and slave mode
- 主机支持的最大通信速率为 fsys/2/ Support communication rate up to fsys/2 under the master mode
- 从机支持的最大通信速率为 fsys/8/ Support communication rate up to fsys/8 under the slave mode
- 可选择自动或手动控制片选 CS 信号的高低/ Automatic or manual control of CS signal
- 独立的发送 FIFO 与接收 FIFO，FIFO 深度为 8 个字，字长度为 4~16 bits(可配置)/ Independent transmission and reception of FIFO, FIFO depth of 8 characters, character length of 4- 16bits (configurable)
- 两路 SPI 互斥，即同一时刻只能一路 SPI 通信/ The two SPI are mutually exclusive, that is, only one SPI communication at the same time
- 当系统进入 Sleep 时，SPI 配置信息将丢失，唤醒后需要重新配置/ Under Sleep mode, the SPI configuration information will be lost, and a re-configuration is required upon system wake-up.

SPI 外设引脚可映射至任意 IO 口。SPI 模块为了和外设进行数据交换，根据外设工作要求，其输出串行同步时钟极性和相位可以进行配置，时钟极性（CPOL）对传输协议没有重大的影响。

SPI peripheral pins can be mapped to any IO port. In order to exchange data with peripherals, the SPI module can configure its output serial synchronization clock polarity and phase according to the peripheral requirements. The clock polarity (CPOL) has no significant impact on the transmission protocol.

- CPOL：时钟极性选择，为 0 时 SPI 总线空闲为低电平，为 1 时 SPI 总线空闲为高电平。/ Clock polarity selection. When it is 0, the SPI bus is idle as low level, and when it is 1, the SPI bus is idle as high level.
- CPHA：时钟相位选择，为 0 时在 SCK 第一个跳变沿采样，为 1 时在 SCK 第二个跳变沿采样。/ Clock phase selection, when it is 0, the sampling is done on the first jumping edge of SCK, and when it is 1, the sampling is done on the second jumping edge of SCK

  不同 CPOL 与 CPHA 配置情况下，其输出波形如图 6-2 至图 6-5 示。

Under different CPOL and CPHA configurations, the output waveforms are shown in Figure 6-2 to Figure 6-5

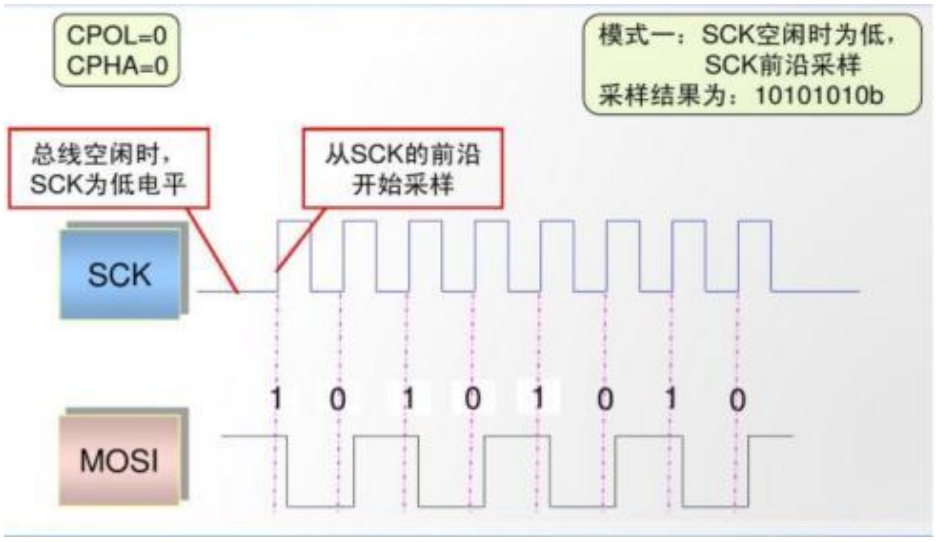


**图 6-2 CPOL=0 CPHA=0**

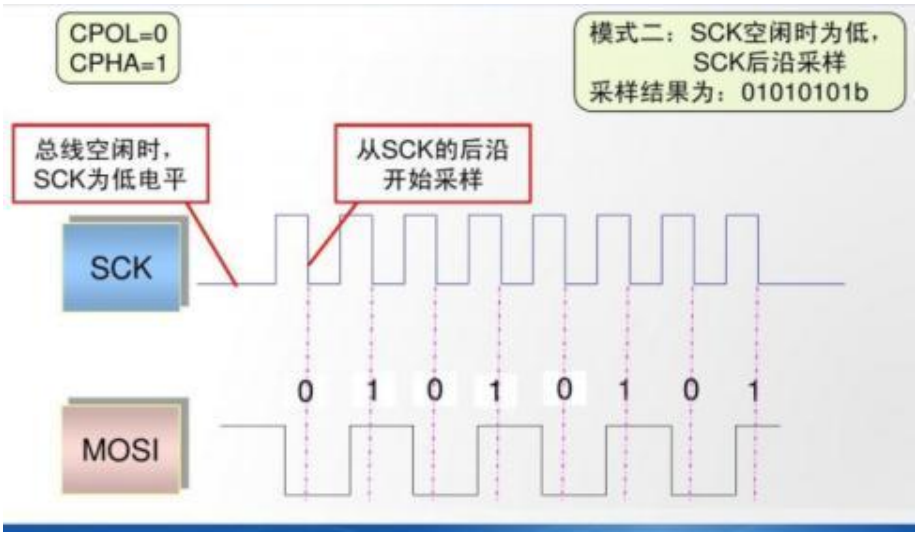


**图 6-3 CPOL=0 CPHA=1**

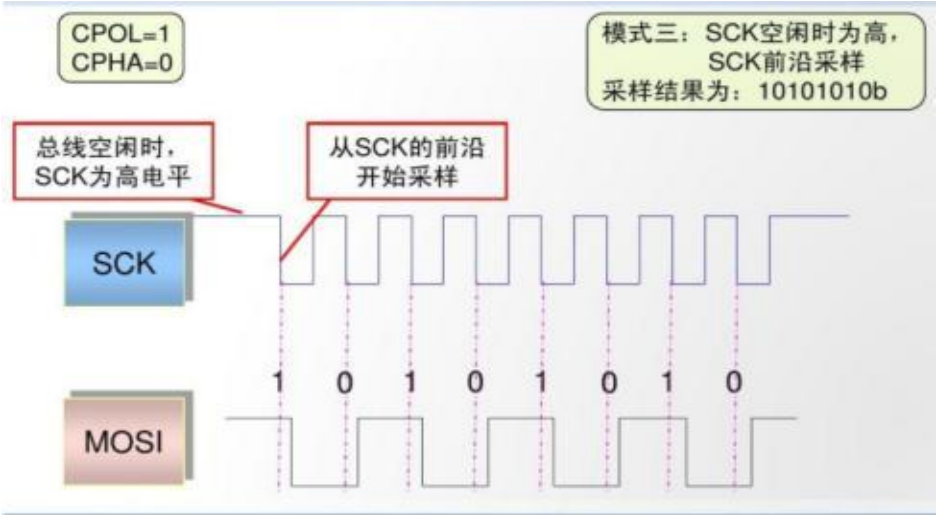


**图 6-4 CPOL=1 CPHA=0**

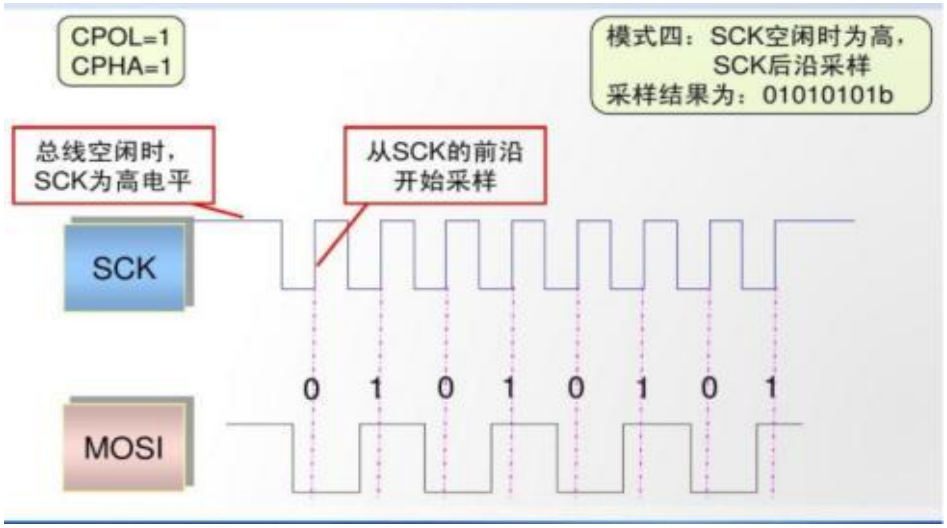


**图 6-5 CPOL=1 CPHA=1**

### 6.2.4 I2C

模块提供 I2C0 与 I2C1 两个外设接口。I2C 模块可以工作在主机模式和从机模式。接口实现了标准模式和快速模式。I2C 接口特性如下：

The chip provides two peripheral interfaces, I2C0 and I2C1, which may work in standard mode and fast mode.

The I2C module can work in master mode and slave mode. The characteristics of the I2C interface are as follows:

- 两线 I2C 接口，包含 SCL、SDA 信号/ Two-wire I2C interface, including SCL and SDA signals
- 支持两种速率模式，标准模式（100Kb/s）与快速模式（400Kb/s）/ Support two rate modes, standard mode ( 100Kb/s) and fast mode (400Kb/s)
- 支持 I2C 主机或从机模式/ Support I2C master or slave mode
- 7 位或 10 位地址寻址/ 7-bit or 10-bit addressing
- 独立的发送 FIFO 与接收 FIFO，FIFO 深度为 8*8bit/ Independent transmission and reception of FIFO, FIFO depth of 8*8bit
- 不支持 I2C 开漏输出/ No supports for I2C open-drain output
- 当系统进入 Sleep 时，I2C 配置信息将丢失，唤醒后需要重新配置/ Under Sleep mode, the I2C configuration information will be lost, and a re-configuration is required upon system wake-up.
- I2C 外设引脚可映射至任意 IO 口。/ I2C peripheral pins can be mapped to any IO port.

### 6.2.5 PWM

模块提供了 6 通道 PWM 输出，可输出频率与占空比可调的方波。PWM 模块特性如下：

The chip provides 6-channel PWM output, which can output square waves with adjustable frequency and duty cycle. The characteristics of the PWM module are as follows:

- PWM 模块时钟频率为 16MHz/ The PWM module clock frequency is 16MHz
- PWM 模块支持预分频，分频系数为：1、2、4、8、16、32、64、128/ The PWM module supports pre-frequency division, and the frequency division coefficients are: 1, 2, 4, 8, 16, 32, 64, 128
- 支持向上计数模式（边沿对齐）与向上向下计数模式（中间对齐）。前者支持占空比 0~100%；后者不支持占空比 0%和 100%，需要 GPIO 输出高低电平来辅助实现。/ Support count-up mode (edge-aligned) and count-up/down mode (middle-aligned). The former supports duty cycle 0- 100%; the latter does not support duty cycle 0% and 100%, and GPIO is required to output high and low levels for assistance.
- 采用 16 位计数器/ 16-bit counter is adopted
- 6 路输出独立配置/ Independent 6-channel output configuration
- 可配置输出极性，输出比较值，顶端值/ Configurable output polarity, output comparison value, top value
- 当系统进入 Sleep 时，PWM 信息将丢失，唤醒后需要重新配置/ Under Sleep mode, the PWM information will be lost, and a re-configuration is required upon system wake-up.

PWM 外设引脚可映射至任意 IO。PWM 向上计数模式与向上向下计数模式输出波形图如图 6-6 与图 6-7 所示。/The PWM peripheral pins can be mapped to any IO. The output waveforms under PWM count-up mode and count-up/down mode are shown in Figure 6-6 and Figure 6-7.

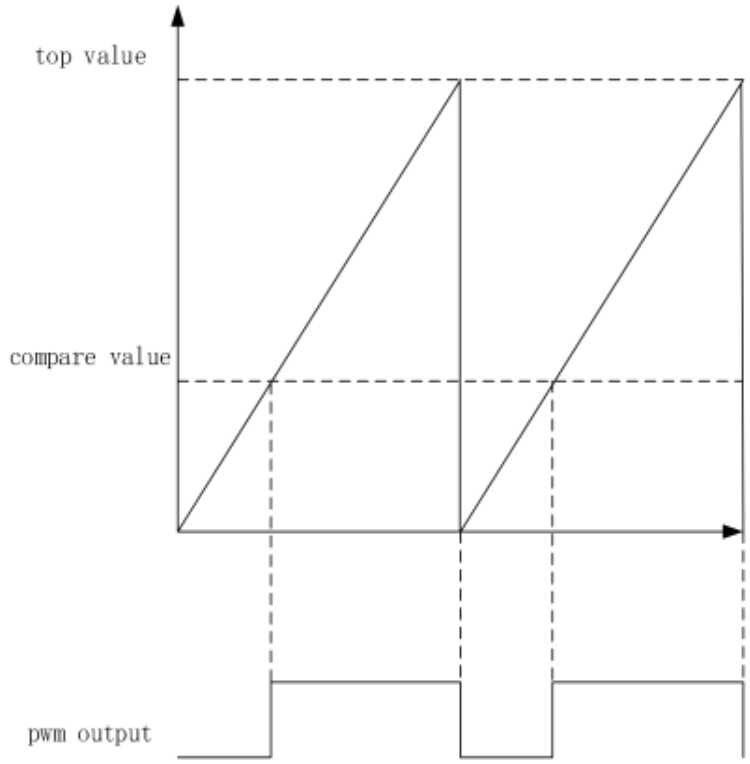


**图 6-6 PWM 向上计数模式/ PWM count-up mode**

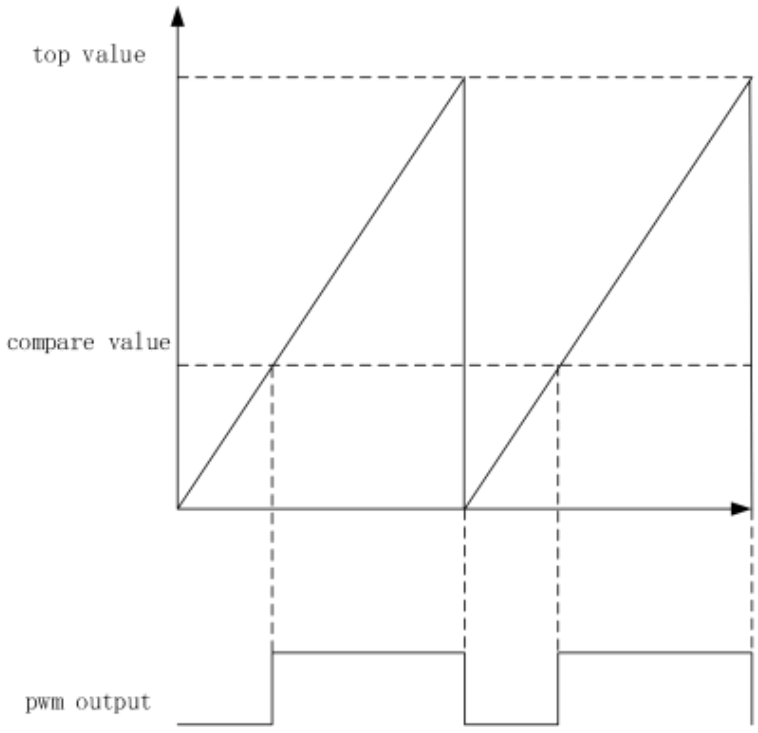


**图 6-7 PWM 向上向下计数模式/ PWM count-up/down mode**

PWM 占空比与频率如表 6-2 所示。/ The PWM duty cycle and frequency are shown in Table6-2.

表 6-2 PWM 占空比与频率/ PWM duty cycle and frequency

| **计数模式/ Count mode** | **占空比/ Duty cycle** | **频率(N 为分频系数）/Frequency (N is the frequency separation factor) N= 1,2,4,8, 16,32,64, 128** |
|---|---|---|
| 向上计数模式/ Count-up mode | CMP_VAL=0 时，DUTY=0; CMP_VAL!=0 时，DUTY=(CMP_VAL+ 1) | 16/N/(TOP_VAL+ 1) |
| 向上向下计数模式/ Count-up/down mode | CMP_VAL/TOP_VAL，Where the CMP_VAL range is：0<CMP_VAL<TOP_VAL | -8/N/TOP_VAL |

PWM 注意事项/PWM precautions：

- 向上计数模式支持频率范围：62.5KHz~8MHz。支持分辨率：0 和 2/65536~65536/65536 /

Under the count-up mode, the applicable frequency range: 62.5KHz~8MHz, applicable resolution: o and 2/65536~65536/65536

- 向上向下计数模式支持频率范围：31.25KHz~4MHz。支持分辨率：1/65535~65534/65535/

Under the count-up mode, the applicable frequency range: 62.5KHz~8MHz, applicable resolution: o and 2/65536~65536/65536

### 6.2.6 ADC

模块集成了 12 位通用 SAR-ADC。ADC 支持 6 路或 3 路单端输入，1 路 PGA 输入。ADC 特性如下：

The chip integrates a 12-bit general-purpose SAR-ADC, supports 6-channel single-ended inputs, and 1-channel PGA input. ADC characteristics are as follows:

- 分辨率 12 位/ 12-bit resolution
- ENOB 10.5bit/ ENOB 10.5bit
- 基准电压为 0.8V/ Reference voltage 0.8V
- 采样率/ Sampling rate
  - 手动模式：默认 80KHz ，同时支持 160KHz 与 320KHz/ Manual mode: 80KHz by default; supports for 160KHz and 320KHz at the same time
  - 自动模式：最大 320KHz 或 256KHz/ Automatic mode: up to 320KHz or 256KHz
- 可支持 6 路或 3 路单端输入，1 路 PGA 输入/ supports for 6-channel single-ended inputs,and 1-channel PGA input

- PGA 通道输入支持 AMIC 单端或差分输入/ PGA channel input supports AMIC single-ended or differential input
- ADC 输入电压范围/ ADC input impedance：
  - 旁路模式/ Bypass mode：0≤Vin ≤0.8V
  - 衰减模式/ Attenuation mode：0≤Vin ≤VDD
- ADC 输入阻抗/ ADC input impedance:
  - 旁路模式/ Bypass mode：＞10MΩ
  - 衰减模式：18.87KΩ (内部采用 14. 15KΩ与 4.72KΩ电阻分压网络，实现信号 1/4 衰减。模块内部电阻绝对误差约为±15%，相对误差约为±1%。绝对误差不影响 ADC 精度，相对误差会影响 ADC 精度。)/ Attenuation mode: 18.87KΩ (The 14.15KΩ and 4.72KΩ resistor divider network is used internally to achieve 1/4 signal attenuation. The internal resistance of the chip has an absolute error of about±15%, and relative error of about±1%. Absolute error will not affect ADC accuracy, while relative error will affect ADC accuracy.)
- PGA 可实现交流信号放大，增益范围 0~42dB，3dB 步进/ PGA can achieve AC signal amplification, with gain range 0~42dB and 3dB step
- 当系统进入 Sleep 时，ADC 配置信息将丢失，唤醒后需要重新配置/ Under Sleep mode, the ADC configuration information will be lost, and a re-configuration is required upon system wake-up.

ADC 的时钟来源于 HCLK，当 HCLK 为 32M、64M 时，ADC 时钟为 1.28Mhz；否则 ADC 时钟为 1Mhz。硬件支持手动模式和自动模式：

The ADC clock originates from HCLK. When HCLK is 32M or 64M, the ADC clock is 1.28Mhz; otherwise, the ADC clock is 1Mhz. Hardware supports manual mode and automatic mode:

1) 手动模式：一次只支持一个单端通道或一组差分采集通道，使其能够采集单端或差分输入信号。

Manual mode: Only one single-ended channel or a group of differential acquisition channels is supported at a time, so as to enable it to collect single-ended or differential input signals.

2) 自动模式：自动扫描所有已启用的多个单端通道，并将转换后的数据存储在相应的内存位置。一次 ADC 采样耗时由 ADC 采样时间和 ADC 转换时间组成，两者均可配，前者是 2T 和 3T，后者 3T 和 2T，T 为 ADC 时钟的周期。

Automatic mode: enabled multiple single-ended channels are automatically scanned, and the converted data is saved in the corresponding memory location. An ADC sampling time is composed of ADC sampling time and

ADC conversion time, both of which can be configured. The former is 2T and 3T, and the latter is 3T and 2T (T is the cycle of ADC clock).

ADC 模块引脚无法任意映射，需要采用固定的引脚，输入引脚配置如表 6-3 所示。

The ADC module pins cannot be mapped arbitrarily and fixed pins are required. The input pin configuration is shown in Table 6-3.

表 6-3 ADC 输入引脚配置/ADC input pin configuration

| 模拟端口/Analog port | 引脚/Pin | 单端模式/Single-ended mode | PGA 模式/PGA mode | 备注/Remarks |
|---|---|---|---|---|
| AIO0 | P11 | √ | | |
| AIO1 | P23 | √ | | |
| AIO2 | P24 | √ | | |
| AIO3 | P14 | √ | | |
| AIO4 | P15 | √ | MIC_PWR | |
| AIO7 | P18 | | PGA_IN+ | |
| AIO8 | P25 | | | |
| AIO9 | P20 | √ | PGA_IN- | |

注意事项如下/Precautions are as follows：

1) 不能同时使用内部分压电阻和外部分压电阻。即如使用衰减模式，外部不要使用分压电阻。

The internal and external divider resistance cannot be used at the same time. That is, external divider resistance cannot be used under attenuation mode.

2) 当要采集的电压较小时，比如小于 0.8V ，也就是在旁路模式量程内，直接使用旁路模式即可。注意采集引脚需要接滤波电容。

For collection of voltage less than 0.8V, i.e. within the range of bypass mode, the bypass mode can be enabled directly. Note that the collected pins need to be connected to a filter capacitor.

3) 当要采集的电压略大时，比如大于 0.8V 但小于 3.2V ，可使用衰减模式或外加电阻分压后的旁路模 式。ADC 精度取决于电阻的相对精度，衰减模式内部相对精度为+- 1%，外部电阻也可以选用+- 1%的电阻。

For collection of voltage greater than 0.8V but less than 3.2V, the attenuation mode or the bypass mode with externally resistive subdivision can be adopted. ADC accuracy depends on the relative accuracy of the resistance. The internal relative accuracy of the attenuation mode is +- 1%, which also applies to the external resistance.

4) 当要采集的电压较大时，比如大于 3.2V ，即超过衰减模式的量程，此时必须采用外部电阻分压后 的旁路模式。注意采集引脚需要接滤波电容。

For collection of voltage greater than 3.2V, i.e. beyond the range of attenuation mode, the bypass mode with externally resistive subdivision is the only choice. Note that the collected pins need to be connected to a filter capacitor.

在采用 ADC 对锂电池电压采样时，通常采用电阻分压的形式。由于衰减模式输入阻抗低，因此不适合电池电压检测，需要采用旁路模式。3.7V 锂电池电压检测推荐电路如图 6-8 所示。

If the ADC is used for lithium battery voltage sampling, the resistive subdivision is adopted in general. The low input impedance under the attenuation mode is not suitable for battery voltage detection and therefore the bypass mode is required. The recommended circuit for voltage detection of 3.7V lithium battery is shown in Figure 6-8.

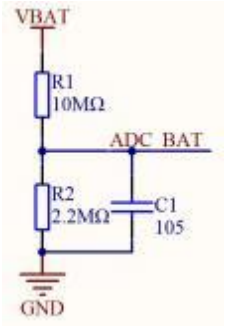


**图 6-7 PWM 3.7V 锂电池电压检测推荐电路/Lithium battery voltage detection recommended circuit**

为了提高 ADC 转换准确性，可从如下方面改进：

In order to improve the accuracy of ADC conversion, it can be improved from the following aspects:

1) 降低 VDD 电源纹波，从而提高内部 ADC 基准 (0.8V) 稳定性。

Reduce VDD power ripple, thus improving internal ADC reference (0.8V) stability.

2) 由于 RF 工作时需要消耗较大电流，将产生较大纹波，因此可以在广播事件或连接事件产生后进行 AD 采样，以便与 RF 错开工作，避免干扰。

RF consumes a large current during operation, resulting in a large ripple. Therefore, ADC conversion can be performed after the broadcast event or connection event, thus avoiding interference.

3) 为了降低 ADC 输入引脚噪声干扰，需要在模块输入引脚并联滤波电容，如 103 电容。

In order to reduce ADC input pin noise interference, it is necessary to parallel filter capacitor in chip input pin, such as 10nF.

4) 对 ADC 原始采样数据进行滤波处理，如 SDK 软件中每 4 笔原始数据进行一次滤波。

Filter the original sampling data of ADC, such as filtering every 4 pieces of original data in SDK software.

# 7. 模组参数 Module Specifications

| 硬件特性/Hardware Features | |
|---|---|
| 模块型号/Model | SKB380 |
| 天线类型/Antenna Type | PCB Antenna/ External Antenna |
| 电压/Voltage | 1.9V~3.6V |
| 尺寸/Dimension(L×W×H) | 17.4×13.7×1.9 mm |
| 无线特性/Wireless Features | |
| 无线标准/Wireless Standards | Bluetooth ® 5.0 |
| 频率范围/Frequency Range | 2.4G-2.4835GHz |
| 数据速率/Data Rates | 1Mbps/2Mbps |
| 无线安全/Wireless Security | AES HW Encryption |
| 传输功率/Transmit Power | Tx Power -20 to +5dBm in 3dB Steps |
| 工作模式/Work Mode | Peripheral (Slave device in BLE connection) |
| 其他/Others | |
| 认证/Certification | ROHS |
| 环境/Environment | Operating Temperature: -40℃~85℃ |
| | Storage Temperature: -40℃~125℃ |
| | 工作湿度/ Operating Humidity: 10%~50% Non-condensing |
| | 存储湿度/ Storage Humidity: 5%~90% Non-condensing |

## 8. PCB 设计参考 PCB Design Guide

请为模组的 PCB 天线预留足够的镂空区域，最小镂空尺寸 16.5*6.6mm，请根据下图 PCB 封装推荐来检查设计是否规范。

Please reserve empty area for PCB Antenna when you are going to design a device`s board, the empty range minimum size :16.5*6.6mm , please kindly check the PCB footprint for reference.

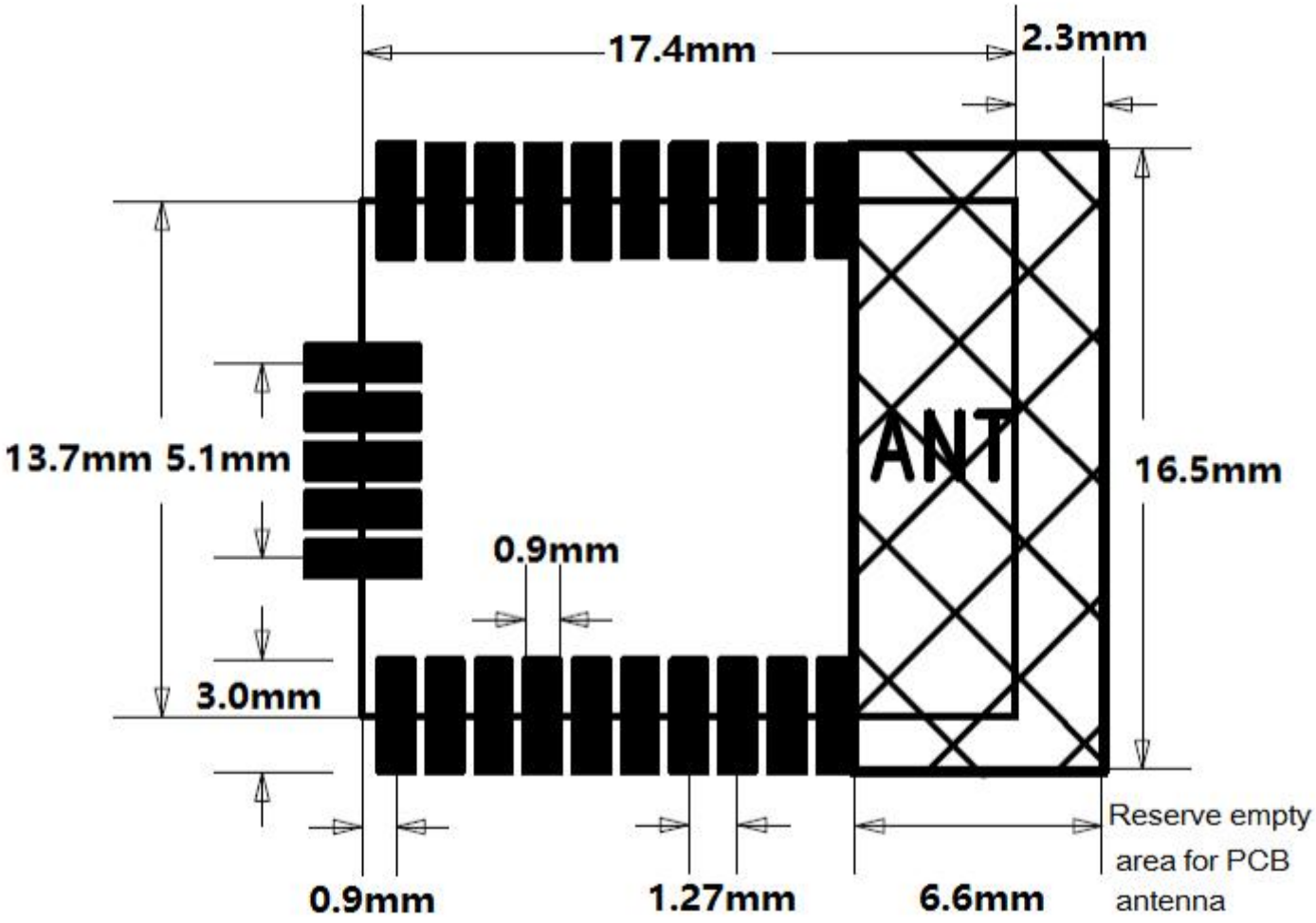


Figure 8　推荐 PCB 封装/ SKB380 Recommended PCB Footprint

# 9. 电气参数 Electrical Characteristics

**极限参数/ Absolute Maximum Ratings**

Table9-1: Absolute Maximum Ratings

| 参数/Parameter | 符号/Symbol | 最小值/Min. | 最大值/Max. | 单位/Uni | 备注/ Note |
|---|---|---|---|---|---|
| Storage Temperature | $T_A$ | -40 | 125 | °C | |
| Operating Temperature | $T_J$ | -40 | 85 | °C | |
| 湿度/Humidity | RH | 0 | 50 | % | Non-condensing, |
| 电源电压/ Supply | VCC | 0 | 3.6 | V | |
| 引脚输入电压 Voltage | $VCC_{IO}$ | -0.3 | VCC+0.3 | V | |
| 湿敏等级 MSL | | | | | MSL3 |
| ESD 放电人体模型 | $V_{ESD-HBM}$ | ≥2000 | | V | |
| ESD 器件放电模型 | $V_{ESD-CDM}$ | ≥500 | | V | |
| ESD 放电机器模型 | $I_{latchup}$ | ≥100 | | mA | |

**推荐参数/ Recommended Operation Ratings**

Table9-2: 运行条件/ Operating Conditions

| 符号/Symbol | 参数/Parameter | 最小值/Min. | 典型值/Typ. | 最大值/Max. | 单位/Uni |
|---|---|---|---|---|---|
| VDD | 工作电源/Power supply | 1.9 | 3.3 | 3.6 | V |
| tr_VDD | 电源上升时间/Power rise time | | | 100 | ms |
| VIH | 数字输入高电平/Digital input high level | VDD-0.7 | - | VDD | V |
| VIL | 数字输入低电平/Digital input low level | 0 | - | 0.7 | V |
| VOH | 数字输出高电平/Digital output high level | VDD-0.3 | - | VDD | V |
| VOL | 数字输出低电平/Digital output low level | 0 | - | 0.3 | V |

**电流/ Current**

Table9-3: 不同状态下的功耗/Power Consumption in Different States

| 参数/Parameter | 最小值/Min. | 典型值/Typ. | 最大值/Max. | 单位/Uni |
|---|---|---|---|---|
| Sleep 模式，32K RTC 运行，SRAM 内容全部保持，可被 RTCtimer 或 IO 唤醒/ In Sleep mode, 32K RTC runs, all SRAM contents are preserved, and can be awakened by RTCtimer or I/o | 4 | 13 | 20 | uA |
| OFF 模式，仅可被 IO 唤醒/ OFF mode: can be awakened only by I/OS | | 0.7 | 3 | uA |
| MCU 运行电流@16MHz ，RF 不工作/ MCU operating current @16MHz, RF does not work | | 3.9 | | mA |
| RX 模式/RX mode | | 8 | | mA |
| TX 模式，0dBm 输出/ TX mode, 0dBm output | | 8.5 | | mA |

Table9-3: RF 特性/ RF Feature

| 符号/Symbol | 参数/Parameter | 最小值/Min. | 典型值/Typ. | 最大值/Max. | 单位/Uni |
|---|---|---|---|---|---|
| Receive sensitivity @ 1Mbps BLE | RF 接收灵敏度@1Mbps BLE | | -93 | | dBm |
| Receive sensitivity@ 2Mbps BLE | RF 接收灵敏度@2Mbps BLE | | -90 | | dBm |
| Maximum input signal level | 最大输入信号强度 | - 10 | -5 | | dBm |
| $P_{TX}$ | RF 输出功率 | -20 | 0 | 5 | dBm |
| $P_{TX}$ Step | RF 输出功率步进 | | 3 | | dBm |
| $F_{req}$ | 频率范围 | 2400 | | 2483 | MHz |

# 10. 生产过程推荐 Manufacturing Process Recommendations

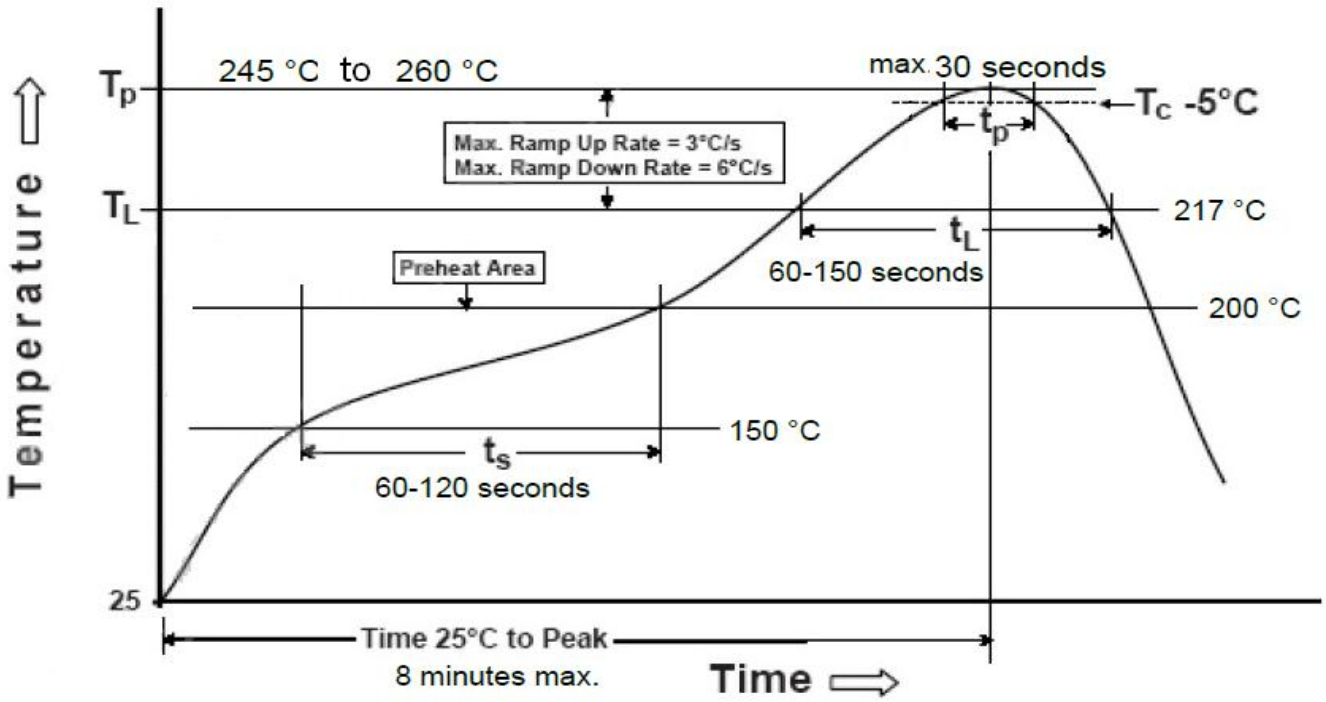


**Figure 10: SKB380 Typical Lead-free Soldering Profile**

**注意：**

1.最终的炉温曲线取决于工厂的其他因素，如锡膏的种类、尺寸、厚度、模组基板的性质等。

2.超出推荐炉温曲线的最高温度可能会损坏模组！

**Note：**

1. The final re-flow soldering temperature map chosen at the factory depends on additional external factors, for example, choice of soldering paste,size, thickness and properties of the module`s baseboard etc.

2. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module！

# 11. 包装信息 Packaging Specification

SKB380 模块放入托盘，每个托盘 528 个单元。每个托盘烘干后真空包装。

SKB380 modules are put into tray and 528 units per tray. Each tray is ‘dry’ and vacuum packaging.

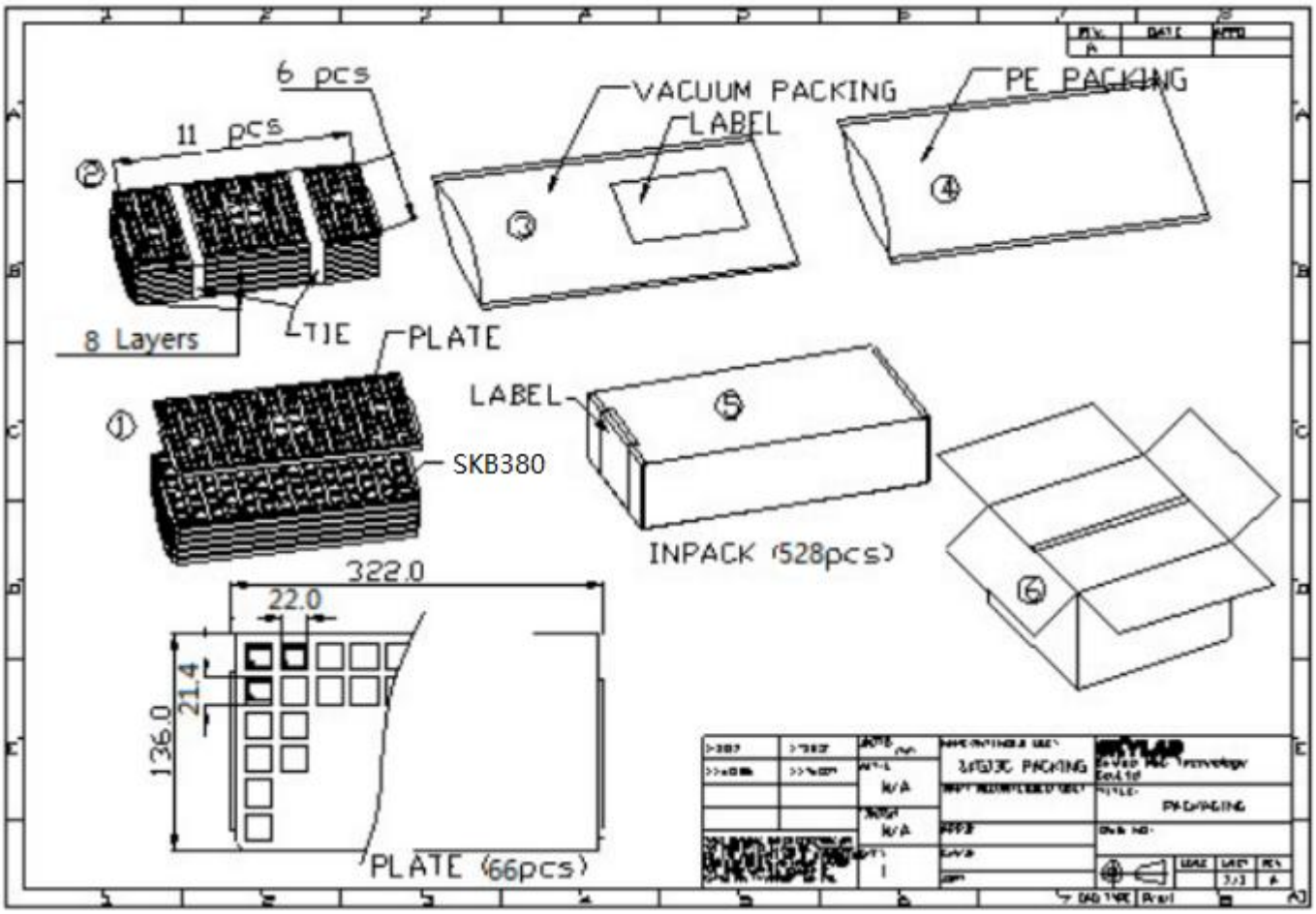


**Figure 11: 包装/ SKB380 Packaging**

# 12. 订购信息 Ordering Information

| Module No. | Crystal | Shielding | Antenna | Temperature Grade |
|---|---|---|---|---|
| SKB380-XXPI | No | No | PCB | Industry |
| SKB380-XXEI | No | No | External (IPEX-III) | Industry |
| SKB380-XSEI | No | Shielding | External (IPEX-III) | Industry |

尾缀含义 Sub-fix definition

**SKB380-ABCD**

| | | |
|---|---|---|
| A | A=C | 支持 32.768kHz 晶体/ 32.768kHz Crystal support |
| | A=X | 不支持/ Not support |
| B | B=S | 支持屏蔽盖/ Sheild cover support |
| | B=X | 不支持屏蔽盖/ Not support |
| C | C=P | 支持 PCB 天线/ PCB antenna |
| | C=E | 外置天线/ External antenna (IPEX-III) |
| D | D | 商用级/ Commercial(0~70℃) |
| | D=I | 工业级=CIndustrial(-40~85℃) |
| | D=V | 车规级/ Vehicle(-40~125℃) |

# 13. 联系信息 Contact Information

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