SKG17MT
规格书/Datasheet

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V1.01	初始版本/Initial Release	Wendy	20220902

Contents

1 General Description

SKG17MT is a GNSS receiver module which supports multiple GNSS systems including GPS, GLONASS and BEIDOU. The 1PPS time pulse is optimized for providing highly accurate timing in the applications which rely on this precision for synchronization and operational efficiency, such as small cell networks, data centers, communication systems and financial networks.

Figure 1: SKG17MT Top View

2 Applications

- 电力高精度授时/High precision timing of electricity
- 个人授时设备/Personal timing equipment
- 基站高精度授时/High precision timing of Base station
- 其他高精度授时/Other high precision timing

3 Features

- Support GPS + GLONASS、GPS + BEIDOU
- 1PPS setting：Pulse width adjustment (default: 100ms)；delay adjustment (range: +/-100ms)
- Antenna supervisor：Antenna short/open/connection indication；Active antenna voltage supply
- Power supply：VCC: 2.8 ~ 4.2V；V_BCKP: 2.0 ~ 4.2V
- Serial interfaces：UART、I2C/SPI
- Time pulse (1PPS) accuracy：1-sigma：< 10ns
- Size：17.0 x 22.4 x 2.4 mm
- Holdover：±3us for 5 minute period
- Timing mode：Survey-in、Position-hold

4 Functional block diagram

Figure 2 shows the functional block diagram of SKG17MT which consists of a single chip GNSS IC, a SAW filter, a TCXO, a RTC crystal, UART/I2C/SPI interfaces, one pulse per second (1PPS) time pulse, and an antenna supervisor including antenna short/open/connection indication and active antenna voltage on/off control from V_ANT supply. Using an active antenna, SKG17MT can achieve the best performance in CNR/TTFF/tracking sensitivity/1PPS timing accuracy.

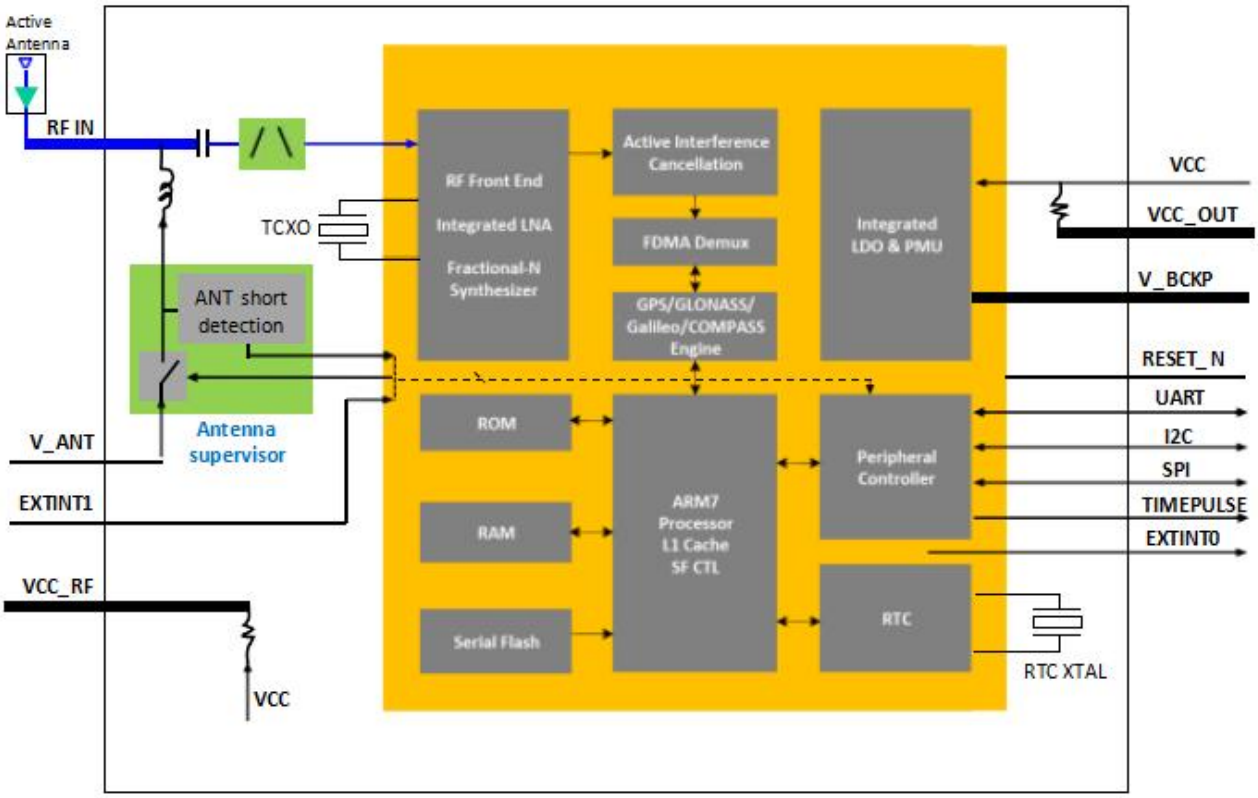

Figure 2 SKG17MT module functional block diagram

5 Timing mode

SKG17MT can support:

- Survey-in
  - A real-time stationary positioning estimated by the receiver and based on the currently available SVs.
  - Based on all available 3D positions and uses a weighted method to estimate the final position.

- A method for determining the final position that is dependent on the requirements of the minimum observation time and the standard deviation (i.e. uncertainty) of the estimated position which is manually set by users.
- When the requirements are met, the receiver uses the final position as the reference position and enters the timing mode.

- Position-hold
  - If the receiver's position is known or previously estimated by the survey-in mode, the corresponding positon can be used as the reference position for the timing mode (i.e. the known position is manually inputted as the reference position for the timing application.)
  - The requirement for the position accuracy, in general, is as accurate as possible. The position error will be translated to the timing error.
- Receiver Autonomous Integrity Monitoring (RAIM) function is used for blunder error residuals detection and measurement exclusion.
- 1-SV timing tracking for poor RF environments (only available in position-hold mode).
- Note:
  - The default setting of SKG17MT is to disable the timing function, which includes the SBAS and QZSS SVs used for aiding purposes and positioning, respectively.
  - When the timing function is enabled, the SBAS and QZSS SVs are excluded from positioning and therefore the timing application.

6 Performance

Table 6-1 Performance (with a good external LNA, Spirent GSS7000)

Item		Test condition	GPS + BEIDOU	GPS + GLONASS
Time pulse accuracy	1PPS 1-sigma	Position hold, 24-hours, >8+8SVs @ -130dBm, C/N0 > 40dB-Hz	< 10 s	< 10ns
Time To First Fix(TTFF)	cold start	-130dBm, Static, >8+8SVs	30 s	30 s
	Hot start	-130dBm, Static, >8+8SVs	1 s	1 s
Sensitivity	Tracking	Cannot lose fixed, Static, >8+8SVs	-165dBm	-165dBm
Current Consumption (VCC=3.0V)	Acquisition	No RF signal input	35mA	34mA
	Tracking	-130dBm, Static, >8+8SVs	38mA	39mA

7 Pin definition

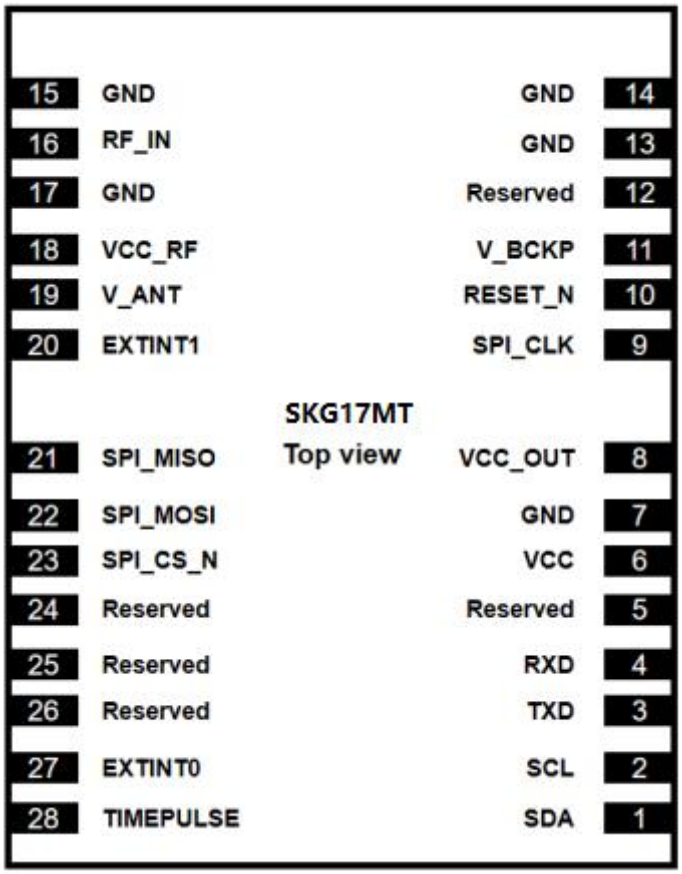

Figure 3 SKG17MT top view

Table 7-1 Pin definition

Pin#	Pin Name	I/O	Description	Remark
1	SDA	I/O	I2C data	2.8V LVTTL
2	SCL	I/O	I2C clock	2.8V LVTTL
3	TXD	O	UART output	2.8V LVTTL
4	RXD	I	UART input	2.8V LVTTL
5	Reserved	-	Not connected	
6	VCC	I	Main supply voltage	2.8 ~ 4.2V
7	GND	-	Ground	
8	VCC_OUT	O	Output Voltage from VCC	
9	SPI_CLK	I	SPI clock	2.8V LVTTL
10	RESET_N	I	System reset	2.8V LVTTL

11	V_BCKP	I	Backup voltage supply	2.0 ~ 4.2V
12	Reserved	-	Not connected	
13	GND	-	Ground	
14	GND	-	Ground	
15	GND	-	Ground	
16	RF_IN	I	RF Input pin	
17	GND	-	Ground	
18	VCC_RF	O	Output voltage from VCC	
19	V_ANT	I	Voltage supply for active antenna	
20	EXTINT1	I	Active antenna status detection	ANT_DEN_N
21	SPI_MISO	O	SPI data output	2.8V LVTTL
22	SPI_MOSI	I	SPI data input	2.8V LVTTL
23	SPI_CS_N	I	SPI control	2.8V LVTTL
24	Reserved	-	Not connected	
25	Reserved	-	Not connected	
26	Reserved	-	Not connected	
27	EXTINT0	I	External Interrupt pin	2.8V LVTTL
28	TIMEPULSE	O	One Pulse Per Second (1PPS)	2.8V LVTTL

8 Electrical Characteristics

8.1 DC characteristics

Table 8-1 Absolute maximum ratings

Symbol	Parameter	Rating	Unit
VCC	Power supply voltage	-0.3 ~ 4.2	V
V_BCKP	Backup battery voltage	-0.3 ~ 4.2	V
ICC_RF	VCC_RF output current	100	mA
V_ANT	Antenna bias voltage	6	V
I_ANT	Antenna bias current	100	mA
TSTG	Storage temperature	-40 ~ +85	℃

Table 8-2 Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Power supply voltage	2.8	3.3	4.2	V
V_BCKP	Backup battery voltage	2	4	4.2	V
VIL	Input low voltage	0	-	0.7	V
VIH	Input high voltage	2.1	-	3.1	V
VOL	Output low voltage	-	-	0.42	V
VOH	Output high voltage	2.38	-	-	V
V_ANT	V_ANT antenna bias voltage	2.8	3.3	5	V
VCC_RF	VCC_RF voltage	-	VCC-0.1	-	V
ICC_RF	VCC_RF output current	-		50	mA
Topr	Operating temperature	-40	25	85	℃

9 Interface Characteristics

9.1 RS-232 interface timing

Required baud rate (bps)	Programmed baud rate (bps)	Baud rate error (%)
4,800	4,800.000	0.0000
9,600	9,600.000	0.0000
14,400	14,408.451	0.0587
19,200	19,164.319	0.0587
38,400	38,422.535	0.0587
57,600	57,633.803	0.0587
115,200	115,267.606	0.0587
230,400	230,535.211	0.0587
460,800	454,666.667	-1.3310
921,600	909,333.333	-1.3310

Note：

1) UART baud rate settings with UART_CLK frequency = 16.368 MHz (UART_CLK uses the system reference clock).

2) The baud rate error is optimized. Each baud rate needs to adjust its counter to obtain the optimized error

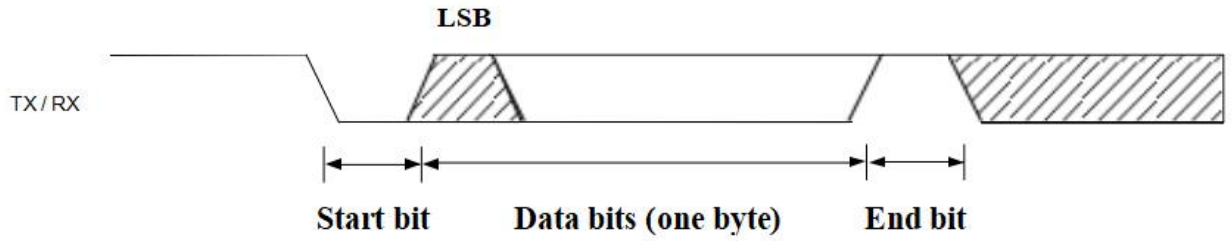

Figure 4 Timing diagram of the RS-232 interface

9.2 SPI interface timing

Description	Symbol	Min.	Max.	Unit	Note
SCS# setup time	T1	0.5T	-	ns	1
SCS# hold time	T2	0.5T	-	ns	1
SO setup time	T3	0.5T – 3t	0.5T - 2t	ns	1, 2
SO hold time	T4	0.5T + 2t	0.5T + 3t	ns	1, 2
SIN setup time	T5	3t	-	ns	1, 2
SIN hold time	T6	10	-	ns	1

Note:

1) The definition of SPI clock cycle (T) is (SPI_IPLL/12) MHz ~ (rf_clk/1,020) MHz.

2) It indicates the period of SPI controller clock, which is SPI_IPLL clock or rf_clk.

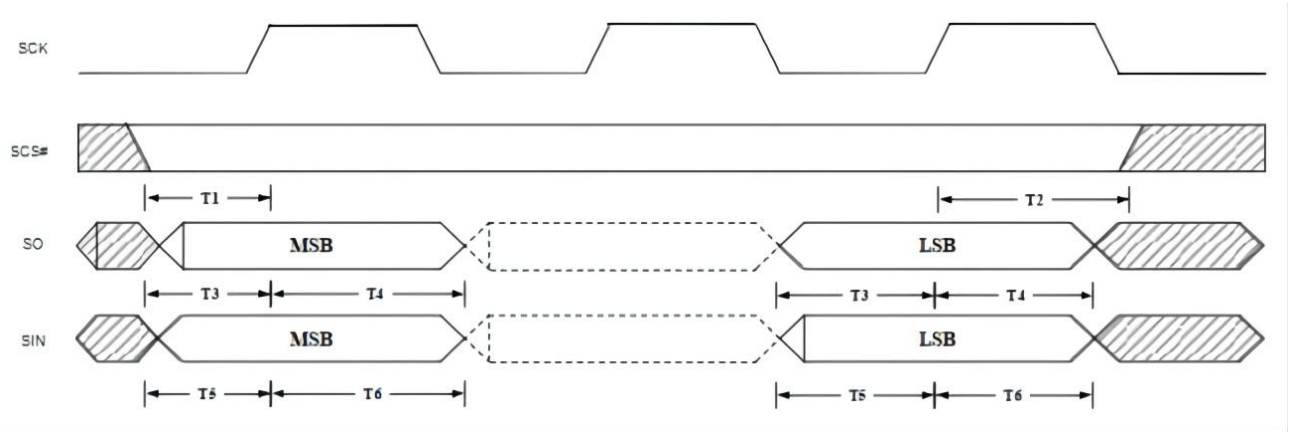

Figure 5 Timing diagram of the SPI interface

9.3 I2C interface timing

Symbol	Period
T1	(MM_CNT_PHASE_VAL0+1)/TCXO_CLK
T2	(MM_CNT_PHASE_VAL1+1)/TCXO_CLK

T3	(MM_CNT_PHASE_VAL2+1)/TCXO_CLK
T4	(MM_CNT_PHASE_VAL3+1)/TCXO_CLK

Note: The condition of I2C clock cycle (I2C_CLK) is (TCXO_CLK/4) MHz ~ (TCXO_CLK/(MM_CNT+4)) MHz. The MM_CNT is the sum of MM_CNT_PHASE_VAL0, MM_CNT_PHASE_VAL1, MM_CNT_PHASE_VAL2 and MM_CNT_PHASE_VAL3 in full speed mode.

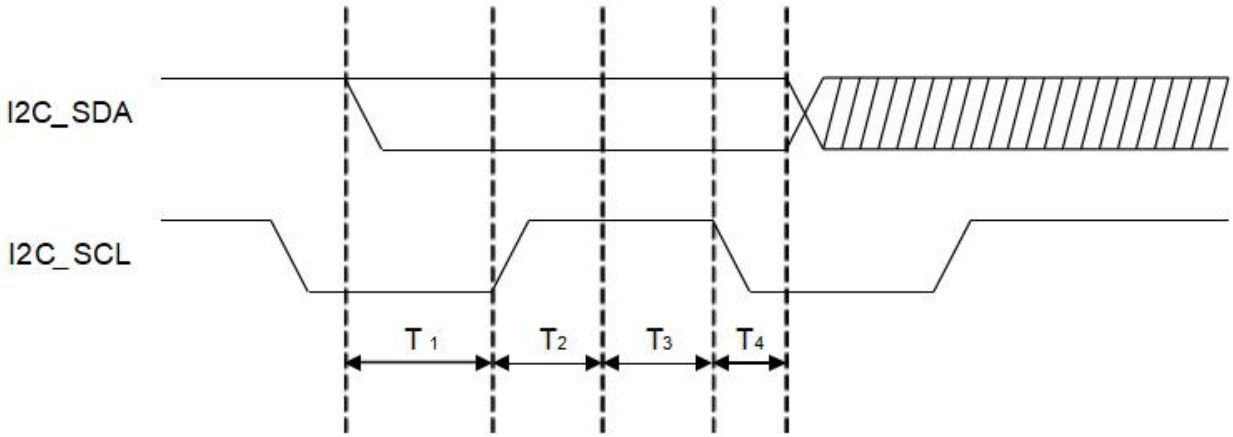

Figure 6 Timing diagram of the I2C interface

10 Mechanical Description

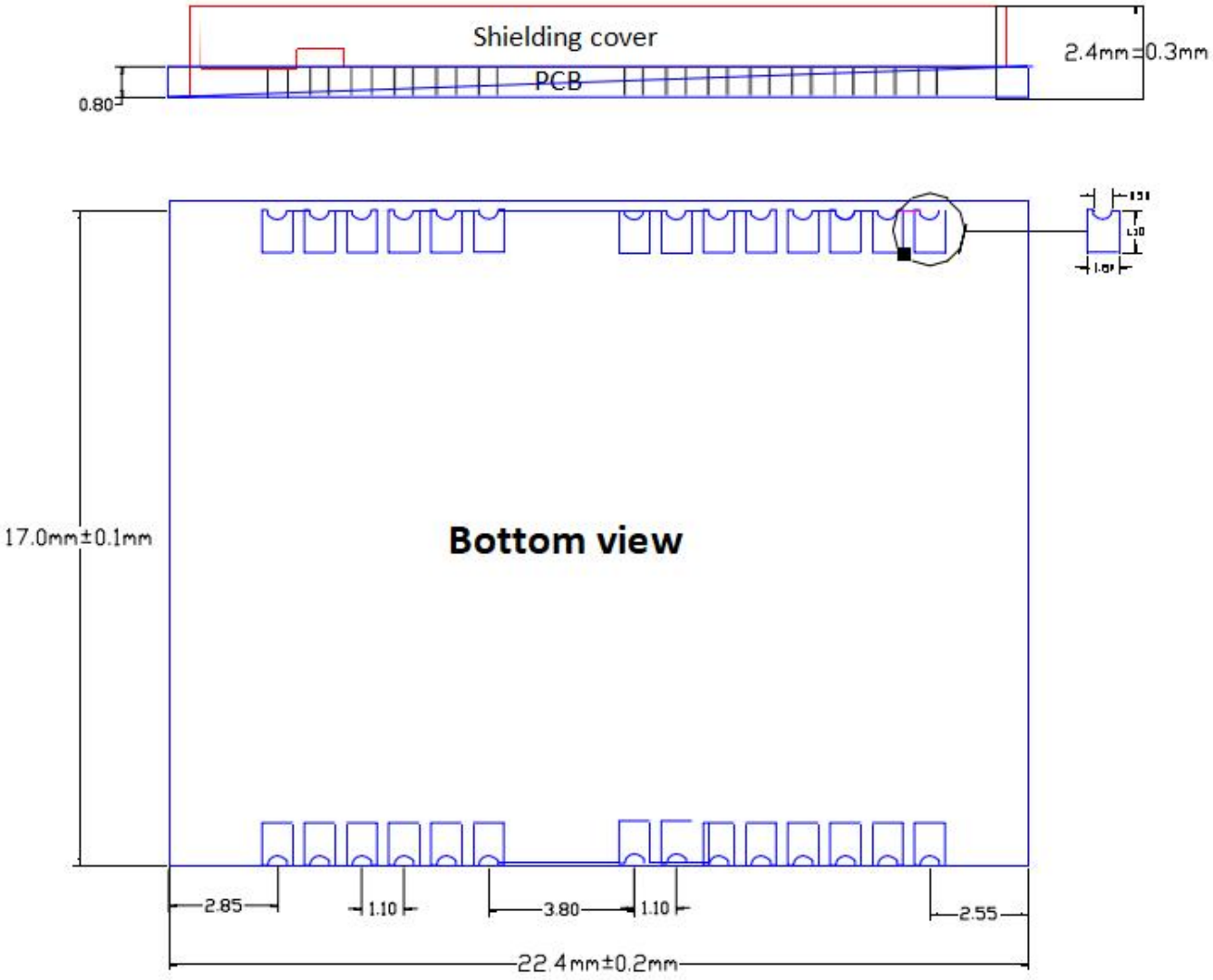

Figure 7 SKG17MT module dimensions

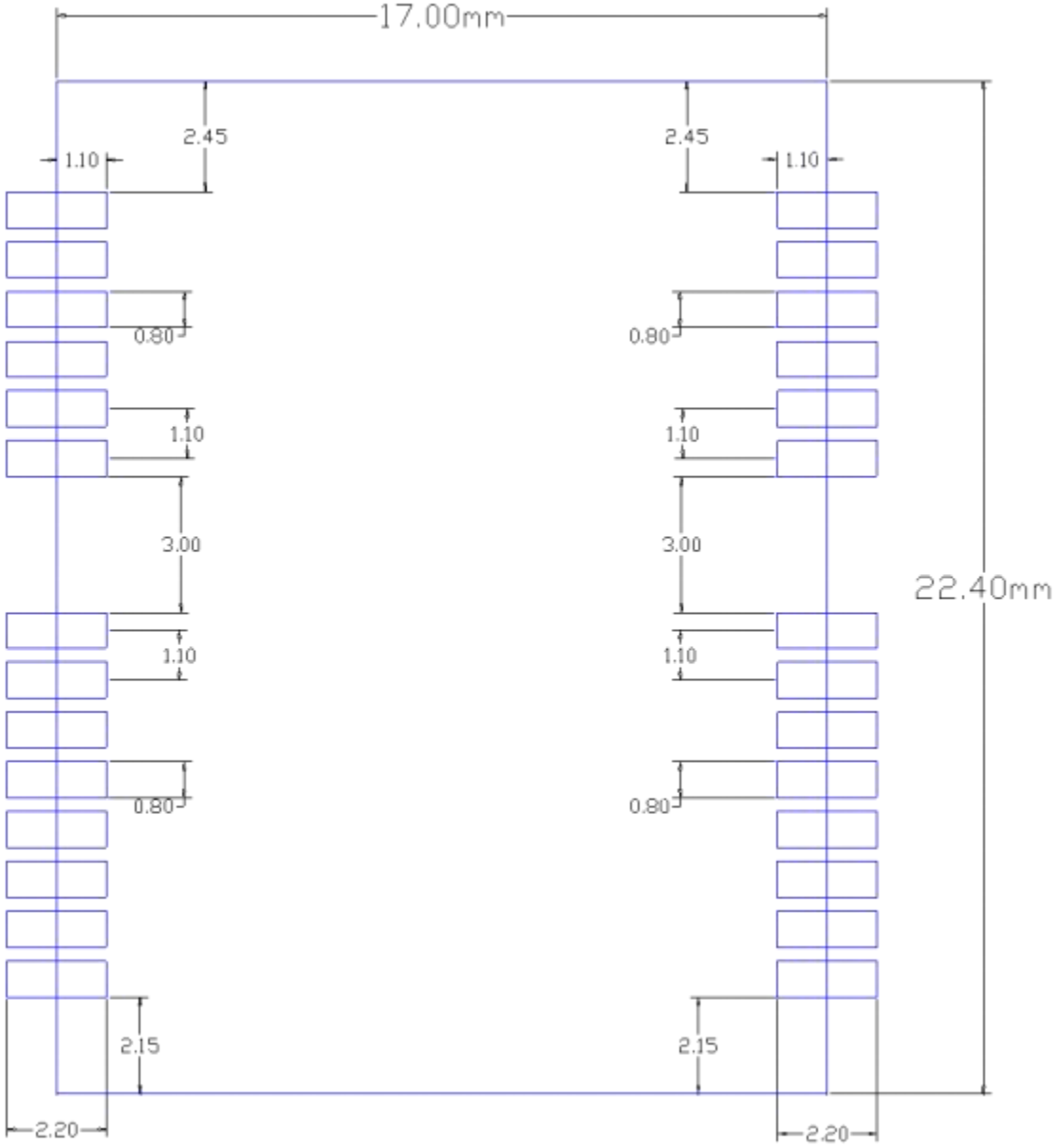

Figure 8 SKG17MT PCB layout footprint

11 Packing specification

SKG17MT are packaged in quantities of 250 pieces on a reel.

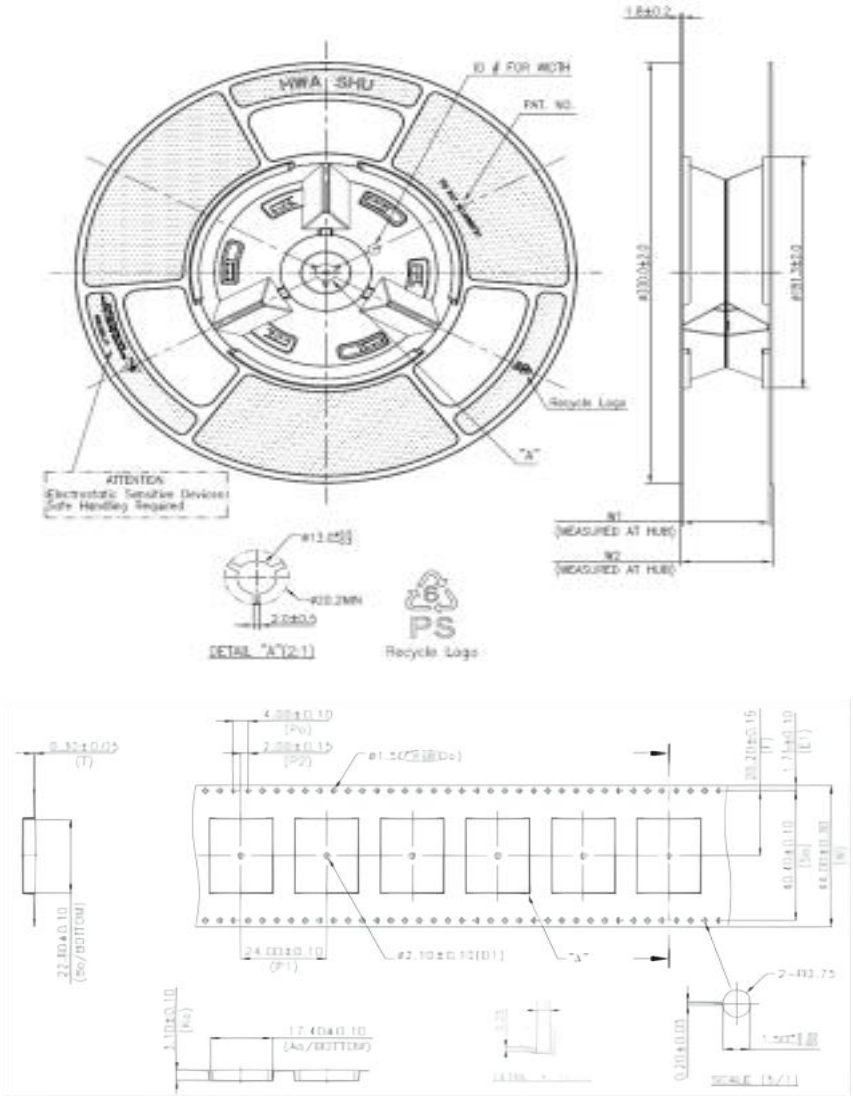

Figure 9 SKG17MT package diagram

12 ESD CAUTION

SKG17MT is an electrostatic discharge (ESD) sensitive device and may be damaged by ESD or spike voltage. Although SKG17MT has built-in ESD protection circuitry, please handle with care to avoid performance degradation or permanent malfunction.

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